

A Scalable 2 V, 20 GHz FPGA using SiGe HBT BiCMOS Technology

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ABSTRACT

This paper presents a new power saving, high speed FPGA design enhancing a previous SiGe CML FPGA based on the Xilinx 6200 FPGA. The design aims at having a higher performance but minimizing power consumption. The new SiGe process has traded off the circuit's performance for reduced power consumption. The power supply voltage has been reduced from 3.4 V to 2.0 V. The structure of the Basic Cell, including the Configurable Logic Block (CLB) and routing multiplexers (MUXs), has been modified so that the supply voltage reduction can be attained. Simulations have shown that the gate delay of the new Basic Cell is reduced from 130 ps in the prior design to 51 ps. The total power consumption for each Basic Cell has been reduced 94% from 71 mW to 4.2 mW, making a large scale FPGA feasible. This design is currently under fabrication for testing.

Categories and Subject Descriptors

B.7.1D.3.3 [Integrated Circuit]: Types and Design Styles – *Advanced Technology, Gate Arrays, VLSI (Very Large Scale Integration).*

General Terms: Design

Keywords

FPGA, CML, SiGe, Basic Cell, CLB.

1. INTRODUCTION

The Field Programmable Gate Array (FPGA) is a configurable circuit consisting of logic blocks surrounded by a programmable routing structure. The structure is shown in Figure 1. The input

signals (A, B and C) are routed through the I/O cells on three different sides to the routing cells, and then passed to the configured logic cell. The routing cells and logic cells are programmed by memories whose data is provided by the configuration file of the CAD software to perform the desired functions. Currently, the versatility of the FPGA has made them useful for networking applications, such as network routers, however the relatively low operating frequency of current commercial FPGAs limits their use in high frequency applications. The Xilinx 6200 FPGA was selected as the blueprint of our design because of its open source structure and the availability of its programming software. Other structures can be implemented if the tools and related information become available.

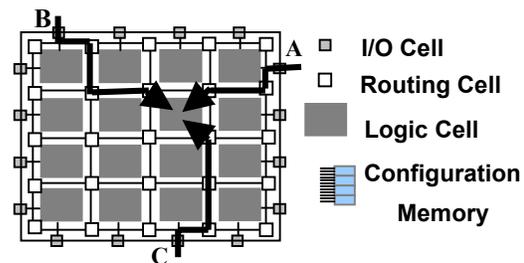


Figure 1. The structure of an FPGA.

In 2000, a SiGe FPGA using Current Mode Logic (CML) was designed that could theoretically approach 20 GHz [1], [2]. CML has several advantages over single ended logic such as immunity to noise and a smaller bias current [3]. Its output is determined by how the current is steered between the differential pairs of inputs. Its high speed characteristic is achieved by operating all transistors out of saturation and keeping the logic swings

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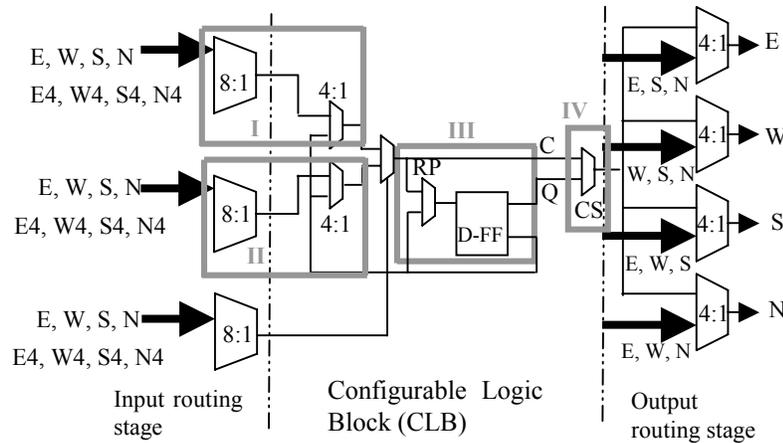


Figure 2. The original Basic Cell structure.

relatively small (250 mV). With breakthroughs in heterojunction bipolar transistor (HBT) technology using SiGe materials, for example IBM's SiGe 5HP process, the gate delay using CML can be reduced to 13 ps.

Since current is always flowing with CML, static power consumption becomes a significant drawback when it is used in low power applications. The problem becomes increasingly severe when CML FPGA designs are scaled up. This paper focuses on how the power consumption is reduced in three ways. First, the power supply voltage is reduced. Second, a trade off is made between the devices' switching speed and tree current. Third, the number of the CML current trees is reduced. This permits a large scale, low power FPGA to be realized.

Section 2 introduces the IBM SiGe 120 GHz BiCMOS Process (7HP), and section 3 describes the new reduced voltage power supply by confining the height of the CML current trees to 2 levels (2.0 V) and reducing reference current by trading off the performance of the device. Sections 4 and 5 introduce the old and new Basic Cells respectively, and describe all the modifications to achieve the goal detailed in section 3. Section 6 explains the programming scheme and routing structure of the FPGA, and section 7 and 8 present the simulation results and the test circuit. The final two sections, 9 and 10, provide insight into future works and summarize the benefits of the new FPGA design.

2. IBM SiGe 120 GHz PROCESS (7HP)

The IBM SiGe BiCMOS process has evolved over several generations through which the HBT's cutoff frequency approaches 120 GHz (for 7HP) and is still increasing (8HP, a 210 GHz process, is under development [4]). Based on the graded Ge alloy base where the Ge content varies linearly across the base to create a built-in electric field, the HBT high frequency performance has caught up with traditional III-V devices such as GaAs. The excellent high frequency performance of the 120 GHz devices has been demonstrated most recently in [5]. With these outstanding high frequency characteristics, logic circuits can be created to operate up to 40 GHz. Our works are based on this technology to boost the performance of the FPGA. In this paper, the simulation results are based on the IBM 8HP design kit which

might help us to predict the best performance of our design. The test chip mentioned later has been fabricated using the IBM SiGe 7HP process.

3. POWER SUPPLY VOLTAGE AND REFERENCE CURRENT REDUCTION

The original FPGA design used a power supply voltage of 3.4 V and a reference current of 0.7 mA. To achieve lower power consumption, both the power supply voltage and reference current were reduced in the new design to 2.0 V and 0.1 mA respectively. Section V further describes how we modify the old circuits in the new one to confine the voltage at 2.0 V. Here, the trade-off between the SiGe devices and the circuits' performances is first described.

The original design was made using the IBM SiGe 5HP process and needed a reference I_c current of 0.7 mA to achieve the ~50 GHz cutoff frequency. The redesigned FPGA uses the 7HP process (120 GHz f_T process), which achieves a ~50 GHz cutoff frequency when the I_c equals 0.1 mA. It is possible to increase the reference current for a significant increase in maximum cutoff frequency. When a 0.1 mA reference current is applied, the power consumption for each CML current tree in the new CLB structure is about 0.2 mW (2 V x 0.1 mA), which is a savings of 92% over the original design.

4. OLD BASIC CELL DESIGN

A reduction in the number of CML trees per Basic Cell results in lower power consumption for the entire device. Therefore, one of the goals is to simplify logic gates of the Basic Cell in the old CML FPGA. The Basic Cell block diagram of the SiGe CML FPGA design is shown in Figure 2. It consists of input/output routing stages and a Configurable Logic Block (CLB). The input routing stage is composed of three 8:1 multiplexers (MUXes) to route the outputs from the surrounding Basic Cells (coming from N, S, E, W) into the CLB. The RP MUX routes the combinational signal and the sequential signals into the D-FF. The CS MUX, which selects combinational or sequential logic, routes the chosen signal to the output stage, consisting of four 4:1 MUXes. The

output routing stage then routes the signals to the neighboring Basic Cells.

5. NEW BASIC CELL STRUCTURE

5.1 Input routing stages in New Basic Cell design.

The redesigned input routing stage combines the logic functions of the 8:1 MUX and 4:1 MUX, shown in the gray blocks I and II of Figure 1 into a new MUX. In Figure 3, the new input routing

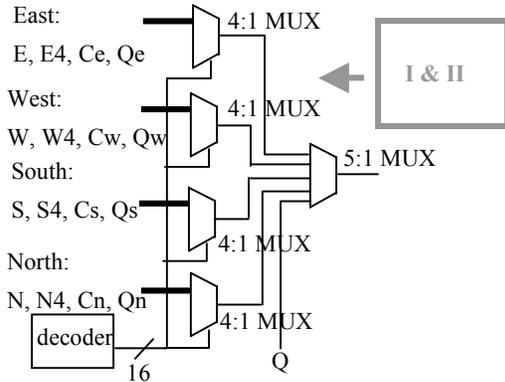


Figure 3. The redesigned input routing stage. Label Ce indicates combinational logic (C) from the east.

stage separates the signals by their incoming directions. All the input signals coming from the same direction (N, S, E, W) are connected to the same 4:1 MUX and only one pair of input signals turns on at a time to route the current through the MUX. The MUX selection is programmed during the configuration of the FPGA. After this configuration, normal operation will not change its selection. For example, all signals originating east of a Basic Cell are connected to one 4:1 MUX. The 8:1 MUX in the original design is broken down into four 4:1 MUXs from all directions, and the 4:1 MUX is combined with the output of the D-FF to become a 5:1 MUX. Advantages of this combination are a reduction in circuit complexity and propagation delay while maintaining full compatibility with the original 6200 configuration bit streams.

The MUXs themselves have been redesigned as well. The general form of the new design is shown in Figure 4. The differential input pair of transistors is connected to the drain of an NMOS switch. Only one pair can be selected in a MUX, so with the use of a decoder the desired differential input pair can be selected and the remaining pairs turned off to save power. The output MUXs have the same MUX configuration.

5.2 Configurable Logic Block (CLB) in the new Basic Cell design.

In block III of Figure 2, the RP MUX was merged into the D-FF, thus further reducing the number of CML trees. Since another input level for the RP selection control is inserted into the D-FF, the CML tree will be taller.

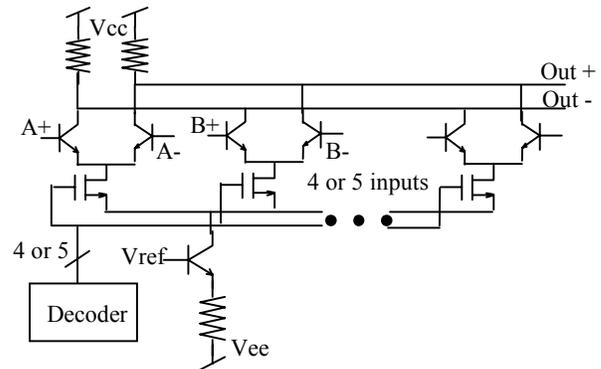


Figure 4. The general form of the new MUX design. The new input routing stage has 4:1 and 5:1 MUXs and the new output routing stage has 4:1 MUXs.

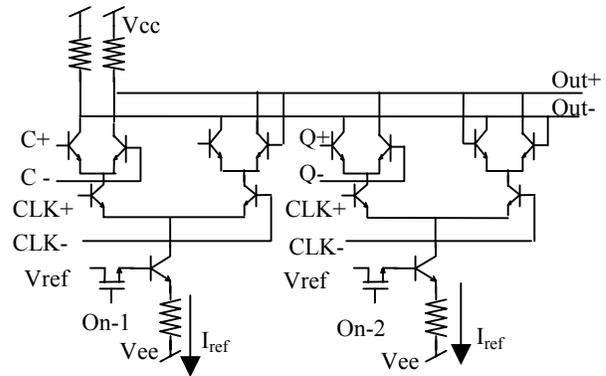


Figure 5. Latch 1 in the new D-FF design.

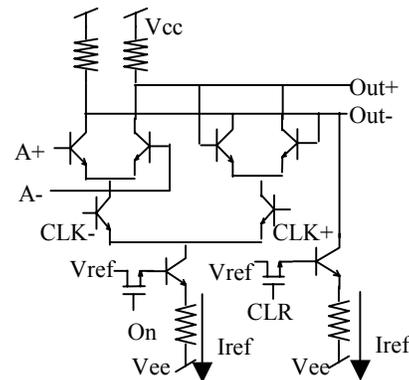


Figure 6. Latch 2 in the new D-FF design.

Reducing the height so that a smaller power supply can be used is crucial. The schematic of the new D-Flip Flop after merging with the RP MUX is shown in Figure 5 for Latch 1 and Figure 6 for Latch 2.

There are methods [6], [7] for designing low power CML digital circuits whose power supply can be reduced to 2.0 V. Their concepts focus on how to properly steer the current into independent current trees. By adding a switch to the Vref transistor in the CML tree, the entire tree can be turned off. In

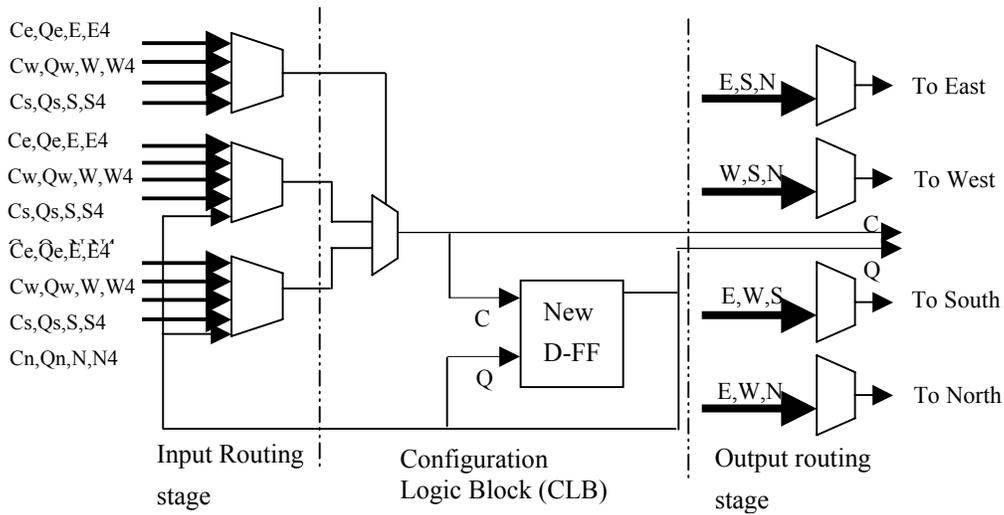


Figure 7. The new Basic Cell. Cx, Qx; x means from “x” direction.

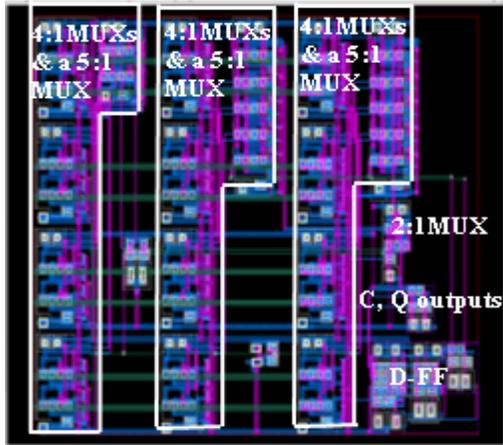


Figure 8. The layout of the new Basic Cell.

Figure 5 showing the Latch 1 design of the new D-FF, we can disable On-2 and enable On-1 if combinational data C (C+/ C-) is the desired input. To select sequential data Q (Q+/ Q-), the On-1 should be turned off and On-2 be turned on. With the use of the switches, the functions of the RP MUX can be completely merged into the first latch.

Latch 2 in the new D-FF design is shown in Figure 6. There are two current trees. However, only one current tree will be turned on at any given time, similar to Latch 1. One is for the D-latch logic and the other is for “CLEAR” (CLR) to directly pull down the output to the lowest voltage in the circuits

The CS MUX, shown in block IV of Figure 2, is used for selecting either combinational logic (C+, C-) or sequential logic in the original design. With the new input stage, this job is now done at the next Basic Cell’s input routing stage, so the CS MUX can be removed from the CLB in the new Basic Cell design to reduce the total gate delay.

The new Basic Cell structure is shown in Figure 7. It is created by simplifying and combining the four blocks (I, II, III and IV) drawn in Figure 2. The overall functions of the Basic Cell remain the same as in the original design to keep the same bit stream and use the existing software (Xilinx 6200) to program them.

After developing the new Basic Cell, the total number of current sources has been reduced from 30 (14 CML trees, 8 pairs of the emitter followers) to 21 (13 CML trees, 4 pairs of emitter followers) and the propagation delay has been reduced as well. The layout of the new Basic Cell is shown in Figure 8.

5.3 Dynamic shut down of unused circuits.

The NMOS switches in every MUX and D-FF can be used to shut down unused portions of those circuits. In the worst case, there will be no circuits that can be turned off except the routing MUXs in the Input stage. The signals from one direction will be picked for the first stage MUXs at the Input stage. Therefore, either the MUXs routing the neighboring Basic Cell or the MUXs routing the neighboring 4x4 Basic Cells will be turned off. There are 21 (13 CML trees, 4 pairs of emitter followers) trees turned on. In the best case, if C (combinational logic C+ and C-) is selected to route to the next Basic Cell and no signals are routed to other Cells, the entire D-FF stage and the Output stage can be shut down. Thus, the number of “ON” current trees is reduced to 9 (7 CML MUXs, one emitter follower pair). Compared to the 30 (14 CML trees, 8 pairs of the emitter followers) trees in the original design, a reduction of 21 current trees is obtained (in the best case).

6. PROGRAMMING SCHEME

In a circuit there is dynamic and static power consumption. In a SiGe CML FPGA, when the dynamic power consumption and static power consumption (CMLs in CLB routing MUXs and decoders) are summed together, the total power consumption will be very large. One source of the dynamic power consumption is from the large CMOS memory cells in the FPGA. The FPGA

should avoid turning on the memory cells and Basic Cells together, to avoid a power surge. To prevent this from happening, a specialized programming scheme has been developed. The programming scheme is composed of two parts. One is the timing scheme and the other is the H programming scheme.

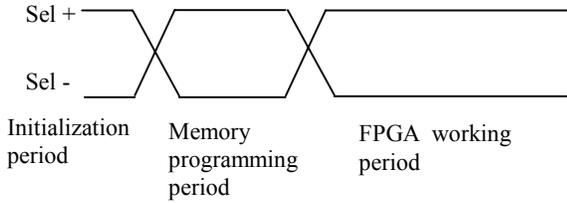


Figure 9. Timing scheme for programming the FPGA

6.1 H-programming structure

How to program the FPGAs is an important issue due to the large amount of memory. To program them, a substantial number of wires are needed to pass the address and data. Those wires create parasitic elements which may cause noisy signals and attenuation. To mitigate these problems, the H-programming scheme is proposed to reduce the number of wires that the circuit needs. This scheme is composed of two parts: the H-programming structure and the memory module.

Figure 10 shows the H-programming structure. The idea originates from the popular H-pattern interconnect structure. During the memory programming period mentioned in the previous paragraph, the Sel (Sel-) will generate the Main-EN to

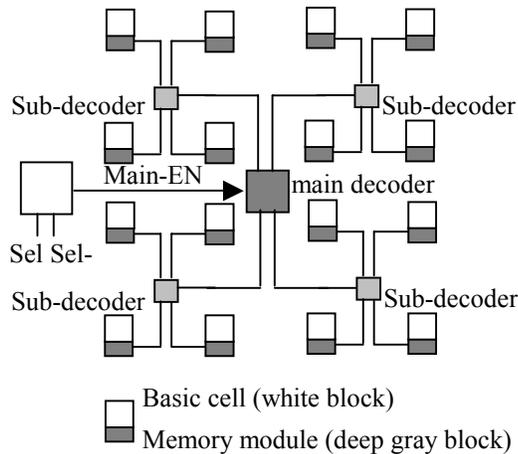


Figure 10. H-programming structure

turn on the main decoder to enable the Sub-decoder in the desired Basic Cells. During the FPGA working period, the main-decoder will generate the CLR signal to clear all the data in the D-FFs.

The memory module is shown in Figure 11 and composed of a data shift circuit and high speed SRAM. During the data write period, the Sel (Sel-) signal will generate Main-EN signal to enable Count-EN. When the counter counts to N, the data is stored in the D-FFs and the counter generates a signal to turn the Counter-EN off. Lastly, the Write-EN is activated and the data

starts to be stored in the memory. During the read period, the Read-EN is on and the data is transmitted to the multiplexers in the Basic Cell.

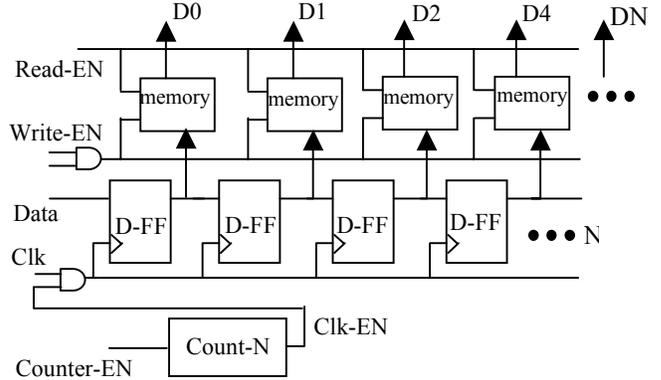


Figure 11. The memory module in the new Basic Cell

This scheme has more clock cycles than other methods; however it greatly reduces the number of interconnect wires that pass the address and data. The parasitic effects due to wire will not be as severe and the size of the FPGA layout can be reduced as well.

7. SIMULATION RESULTS

All of the MUXs in the Basic Cell are programmed during configuration and remain in that mode during operation. The simulations were done based on the following specifications shown in Table 1, which compares the basic electrical properties of both the 5HP and 7HP designs.

Table 1. The processes and electrical properties of the old and new Basic Cell

	Process	Vcc, Vee (V)	Reference current (mA)	current trees
Old design	IBM SiGe 50 GHz (5HP)	Vcc=0 Vee=-3.4	0.7 mA	30
New design	IBM SiGe 210 GHz (8HP)	Vcc= 0 Vee=-2.0	0.1 mA	21

7.1 Power consumption

A constant current is always flowing through the CML tree. There is only static power consumption which is not influenced by the operating frequency. Assuming the CML trees in the Basic Cell are on, the power consumption of each new Basic Cell is about 4 mW (without considering the dynamic shut down method). In the prior design the power consumption was 71.4 mW (3.4 V x 0.7 mA x 30). Thus for each Basic Cell, 94% power is saved. This is a

savings of 2% more than the design with only the reduced voltage and reference current.

7.2 Propagation delay and rise/fall time

The simulation results show that the gate delay, which is defined by the time that signals propagate to the output of the new Basic Cell, is about 51 ps. Compared to the 130 ps delay of the prior design, the gate delay of the new design is reduced by 60%. The power and gate delay data was collected and shown in Figure 12. The cylindrical bars indicates the power consumption and the rectangular bars indicate the gate delay.

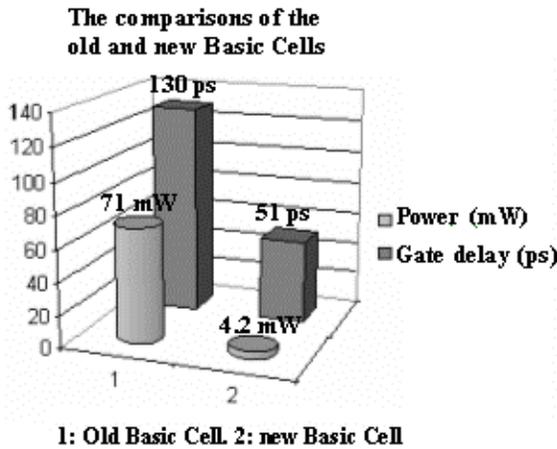


Figure 12. The power consumption and gate comparison of the old and new designs.

The measurement of the rise/fall time of the Basic Cell is based on the AND logic simulation result with the time difference between the 10% and 90% of the output voltage for the rising edge and 90% and 10% for the falling edge. The new Basic Cell design has a rise time of 55 ps and a fall time of 40 ps with 6 Basic Cells loaded. The prior design has 71 ps rise time and 82 ps fall time with 4 Basic Cells loaded. The results are collected and shown in Figure 13.

7.3 Logic verification

Since the Basic Cell has been modified, the cell's functions need to be verified. Each Basic Cell can perform one logic operation on two inputs (A and B). The input signal A of the test simulations is a square wave with period of 1.4 ns and input B is set at 1 ns. The Basic Cell was programmed as an AND, OR and XOR gate. The resulting waveforms are shown in Figure 14 a, b and c. The waveforms below verify that the Basic Cell is performing the correct operation.

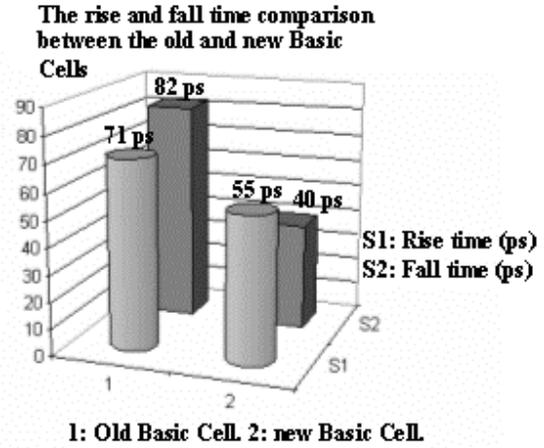


Figure 13. The rise time and fall time simulation results.

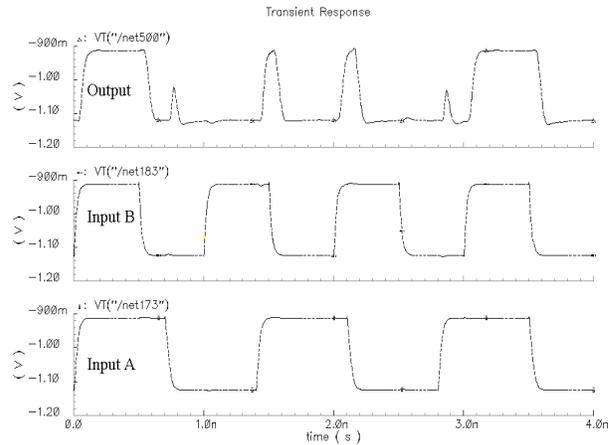


Figure 14a. The AND logic simulation result of the new Basic Cell design. (Input A period: 1.4 ns. Input B period: 1 ns.)

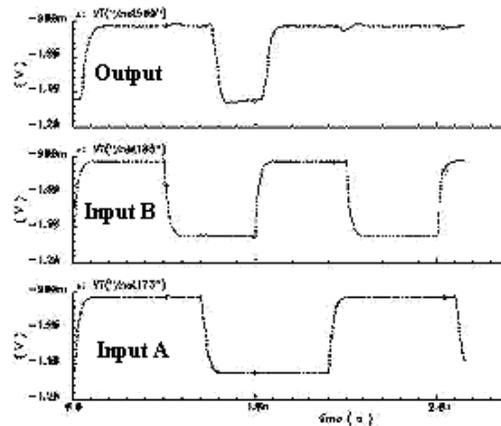


Figure 14b. The OR logic simulation result of the new Basic Cell design.

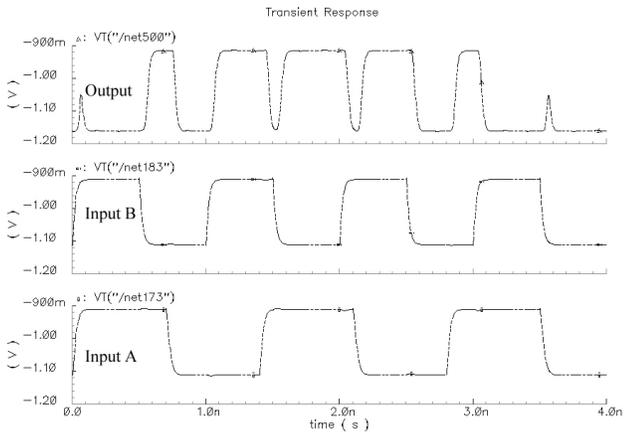


Figure 14c. The XOR logic simulation result of the new Basic Cell design.

8. TEST CIRCUIT

The existing test layout, micrograph and measured output waveform are shown in Figure 15, 16 and 17. The purpose of this test circuit was to confirm the logic functionality and speed of the early CLB design. It consists of a CLB unit and a ring oscillator set to run at 5 GHz. The CLB unit is programmed to be a buffer, and the ring oscillator was used as the input waveform.

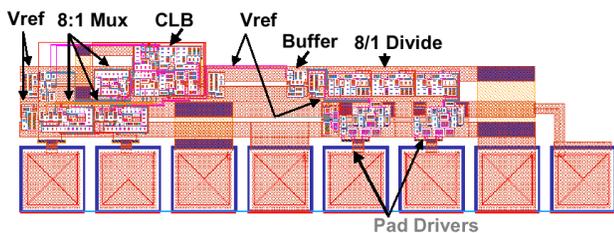


Figure 15. The layout of the prior CLB test chip.

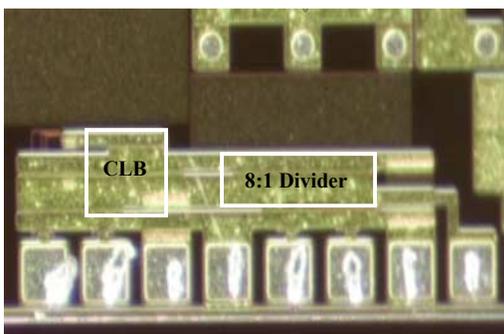


Figure 16. CLB test circuit micrograph.

The primary goal of the new test circuit is to determine the maximum speed of the new Basic Cells in an FPGA. To achieve this measurement, four neighboring new Basic Cells are serially connected through the routing MUXs by programming the output routing stage in a ring oscillator fashion, with the first output of the Basic Cell inverted. The layout of the Basic Cell ring

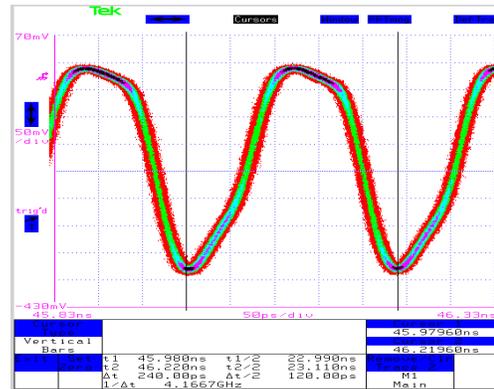


Figure 17. CLB test circuit output waveform.

oscillator test circuit is shown in Figure 18 based on the IBM 7HP process. It contains two different speed ring oscillators. The one on the left hand side of Figure 18 has a higher reference current ($I_{ref} = 1 \text{ mA}$) to achieve higher operation speed. The other block on the right hand side of Figure 18 is the slower speed, power saving one with lower reference current ($I_{ref} = 0.1 \text{ mA}$). Details of the oscillators are shown in Figure 19a and 19b. The simulation results in Figure 20a and 20b show the sinusoidal waves with a period of 370 ps, or 23.6 GHz for the higher speed case and 1.1 ns (7.2 GHz) for the lower speed power saving case.

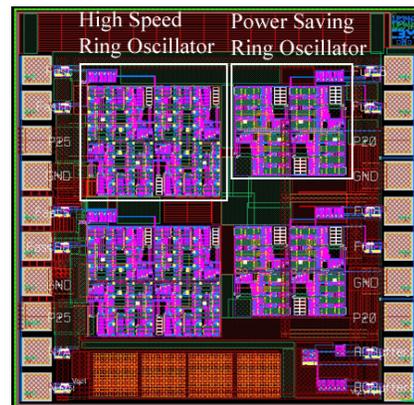


Figure 18. The test chip layout. (four-stage Basic Cell ring oscillators.)

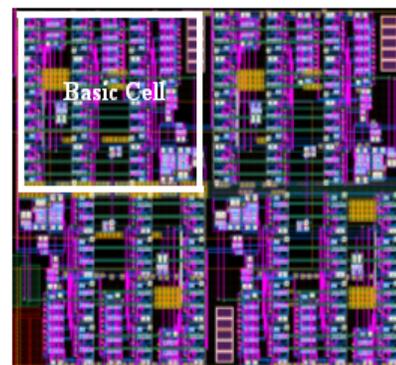


Figure 19a. The layout of the high speed four stage Basic Cells ring oscillator (left hand side block of Figure 12).

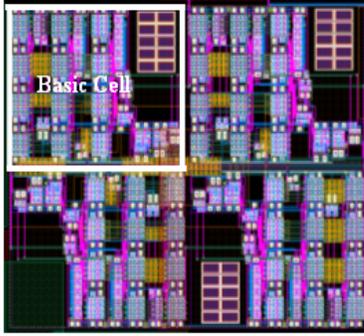


Figure 19b. The layout of the low speed four stages Basic Cells ring oscillator (right hand side of Figure 12).

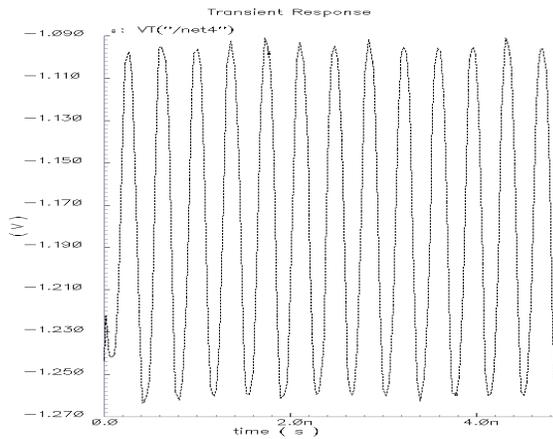


Figure 20a. The high speed four stages Basic Cells ring oscillator with period of 350 ps.

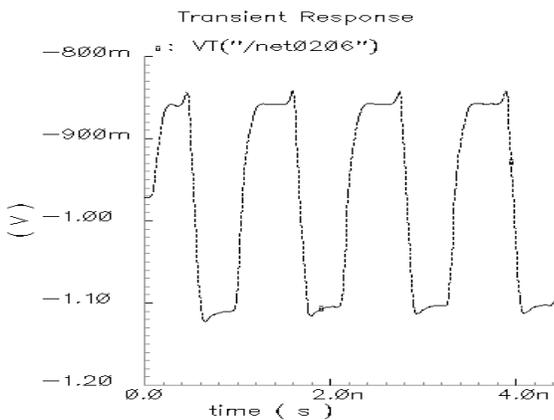
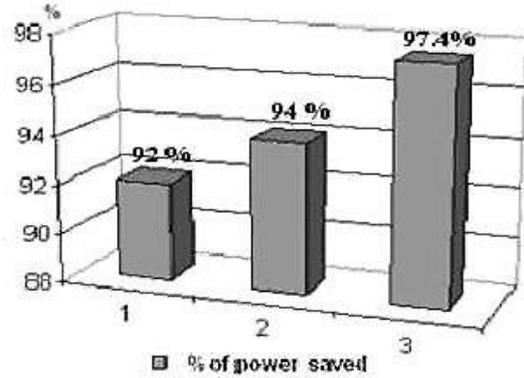


Figure 20b. The low speed four stages Basic Cell ring oscillator with the period of 1.1 ns.

9. SUMMARY AND FUTURE WORKS

Several methods were used to reduce the power consumption of the Basic Cell. The first method, reducing power supply from 3.4 V to 2.0 V, accounts for most of the saved power, a total of 92%. The second method, combining and simplifying the logic of the

old Basic Cell, has reduced the number of current trees by 9, from 30 to 21. It contributes another 2% power saving, saving 94% power (compared to the old design). The dynamic shut down of unused circuits reduces more trees from 21 to 9, saving 97% more power than the old design. The last method depends on the routing situation, and can save up to 21 current trees. The percentage of power saved for the above strategies are plotted and shown in Figure 21.



- 1: power supply voltage reduction
- 2: Power supply voltage reduction and new Basic Cell design
- 3: Power supply voltage reduction and new Basic Cell design and dynamic shut down method

Figure 21. The percentage of the total power saved by the power saving strategies.

The new Basic Cell design has been submitted for fabrication at IBM. After the finished product is received, the logic functions can be confirmed. Future work will involve a scale up of the new FPGA design to sizes required by communications and DSP applications.

10. CONCLUSION

The aim of this work is to maximize the power savings of the original FPGA design while maintaining the logic structure and performance. For the new IBM process, three methods and a programming scheme to reduce power have been used and have shown to provide significant power savings over the original design. With the reduced power consumption we can now scale the FPGA to a 64x64 Basic cell array making it viable for more high speed applications.

11. ACKNOWLEDGMENT

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