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A 10 GHz 4:1 MUX and 1:4 DEMUX implemented by a Gigahertz SiGe FPGA for fast ADC

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Abstract

This paper describes the implementation of a scalable SiGe FPGA that serves as an interleaving and de-interleaving block in a high-speed reconfigurable data acquisition system. In this paper, the different generations of SiGe configurable blocks (Basic Cells(BC)) evolved from the Xilinx 6200 are presented and measured. The latest generation has a 94% reduction in power consumption (from 71 to 4.2 mW) and an 82.5% reduction of the propagation delay (from 238 to 42 ps) compared to the first generation design. To demonstrate the SiGe FPGA's capabilities of handling gigahertz signals, the SiGe FPGAs configured as the 4:1 multiplexer and 1:4 demultiplexer were designed to run at 10 Gbps. The comparisons between the SiGe and CMOS FPGAs are also provided. With these design results, the SiGe FPGA is able to process gigahertz signals such as S and K microwave bands.
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Keywords: FPGA; Reconfigurable; SiGe; Mux; Demux; 10 GHz

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1. Introduction

Field programmable gate arrays (FPGAs) are now widely used for the implementation of digital systems. They were first introduced by Xilinx Inc., San Jose, CA, and have demonstrated their versatility in many fields such as networking and digital signal processing (DSP). Commercial FPGAs are generally limited by the use of CMOS, and hence have low operating frequencies in the sub-gigahertz range. There are many applications that can benefit from the use of high speed FPGAs, which is obtainable through the use of current bipolar technologies. Due to the excellent high-speed performance of Current Mode Logic (CML), it is the architecture of choice for implementing an FPGA configurable block running at gigahertz frequencies. In 2000, the first high speed SiGe FPGA utilizing CML and running in the gigahertz range was proposed [1,2]. This has opened a window to gigahertz configurable applications.

A high-speed reconfigurable system is proposed to process such high-frequency signals. By inserting a SiGe FPGA between the high-speed front end and a CMOS FPGA and after the CMOS FPGA before the high-speed back end, the gigahertz signals can be fully interleaved and de-interleaved. This mixed configuration takes advantage of the high speed of a SiGe FPGA and the low power and high complexity of a CMOS FPGA. To demonstrate the capability of a SiGe FPGA applied to the proposed system, the SiGe FPGA is programmed to be a 4:1 multiplexer (MUX) and 1:4 demiltiplexer (DEMUX). To be compatible with a high speed ADC that runs at 20 GHz, the 4:1 MUX and 1:4 DEMUX must have a 10 Gbps transmission rate. To achieve this, a modified FPGA structure with less propagation delay and power consumption was proposed in 2002 [3]. The propagation delay and power consumption of the new SiGe FPGA have been greatly reduced. This paper is an extension of work presented at the Great Lake Symposium on VLSI 2004. It includes more circuit details and measurements, such as comparisons of different generation SiGe FPGAs (Section 3.1), simulations of the 4:1 MUX and 1:4 DEMUX (Section 4), and comparisons of transmission rate and power consumption for SiGe FPGA and CMOS FPGA (Section 5).

Sections 2 briefly describes why SiGe technology is used and its advantages in high-speed applications. It also introduces the proposed high-speed reconfigurable system that works for gigahertz applications and the role of the SiGe FPGA in it. Then the proposed FPGA configurable cell (Basic Cell (BC)) and its performance are described in Section 3. Measurement results of previous BC test chips are also presented here. In Section 4, a prototype high-speed reconfigurable system used to process acquired data is provided as an example. As a critical functional block, the SiGe FPGA implements a 4:1 MUX and 1:4 DEMUX to demonstrate its capability to handle gigahertz signals. Simulation results of the MUX and DEMUX have been compared to CMOS FPGAs and summarized in Section 5. Lastly, Section 6 presents the conclusion and future work is discussed.

2. High-speed reconfigurable system implemented by the IBM SiGe processes

Technical progress in bringing SiGe HBT technology to reality has been exceptionally rapid. The SiGe HBT has demonstrated ability to provide excellent high-performance characteristics with very low noise, at high power gain, and with excellent linearity, all providing designers wide

latitude in solving challenges for specific requirements [4]. With the graded Ge doping in the base, the base band structure has been changed by introducing a quasi-electric field that drives the electrons across the base [5]. The IBM SiGe BiCMOS process has evolved over several generations, resulting in the HBT's cutoff frequency approaching 120 GHz (7HP—high performance). A 210 GHz process (8HP) has just been released and the news of 350 GHz (9HP) process has been reported [6]. Fig. 1 shows the cutoff frequency of the 0.5 and 0.25 μm processes (5HP) is around 47 GHz [7]. The 0.18 μm process (7HP) reaches 124 GHz [7]. The excellent high-frequency performance of the 120 GHz devices has been demonstrated most recently [8]. Using these, SiGe logic circuits can be created to operate at 40 GHz. One useful characteristic about the SiGe HBT worth noting is that if fast device switching speed is not necessary, it is possible to trade its excess speed for reduced power consumption. It can be observed from Fig. 1 that the f_T of the IBM next generation (8HP) is about 1.75 × faster than the 0.18 μm (7HP) process. The collector current of the 8HP process has the same f_T as the maximum f_T of 7HP while it is 10 × smaller than that of 7HP [4]. This strategy is utilized in the high-speed, low-power FPGA design.

As the amount of data processed and transferred between systems ever increases, the need for complex functions and fast throughput of digital systems rises as well. To solve this problem, higher operating frequencies are needed. Conventional CMOS FPGAs are widely used in data processing areas. They have several advantages over bipolar FPGAs such as higher transistor density and lower power consumption, however most of them can only run up to several hundred megahertz, which limits their use in gigahertz applications (S band, K band, etc). A high-speed reconfigurable system is proposed in Fig. 2. By inserting a SiGe FPGA between the high-speed front and back ends and the low-speed CMOS FPGA, the operating frequency required by the CMOS FPGA can be diminished. The high-speed front-end and back-end operate at frequencies of 10–80 GHz. A SiGe FPGA operating in the range of 500 MHz – 10 GHz can interleave or

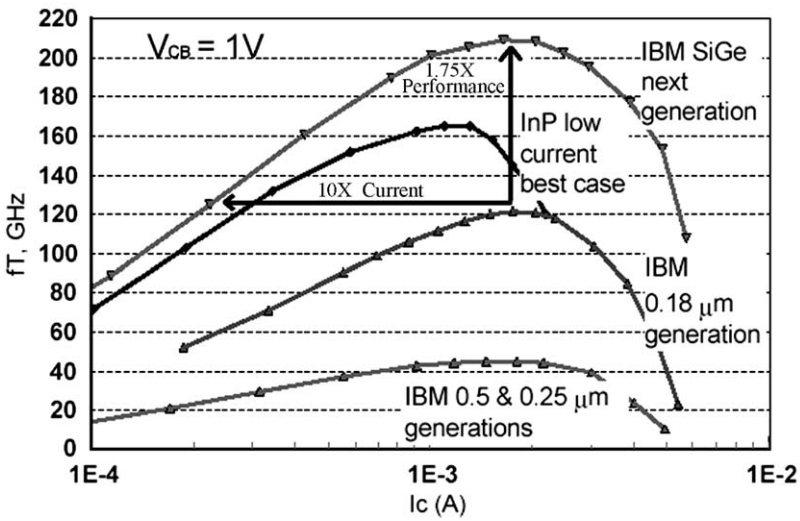

Fig. 1. Cutoff frequencies of several generations of SiGe processes [7].

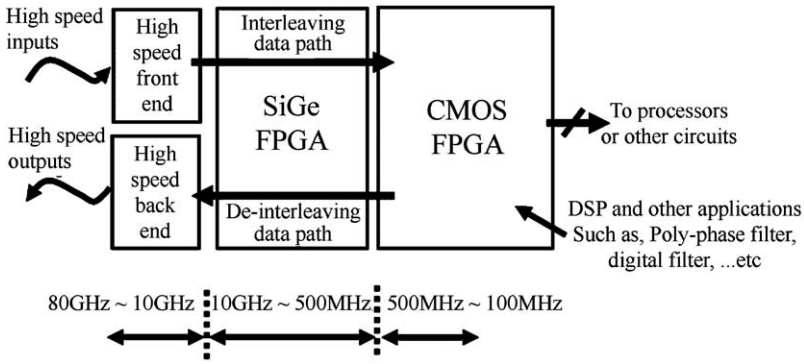

Fig. 2. Proposed high-speed reconfigurable system.

pre-process the signals from the high-speed front-end for the CMOS FPGA and de-interleaves the CMOS FPGA's outputs for the high-speed back-end. Thus, the high-frequency signals may be processed by the CMOS FPGA where more complex processing functions can be implemented. In the proposed system, the SiGe is the key technology for lowering the operating frequency required by the CMOS FPGA.

The SiGe FPGA is implemented in Current Mode Logic (CML). It is the second generation of Emitter Coupled Logic (ECL). Like ECL, it is a differential logic design methodology that focuses on steering instead of switching currents on and off. It has many similarities to ECL design, such as preventing the transistor from saturating and wide use of emitter coupled differential pairs. Several advantages have been described [9]. Overall, less power is consumed with CML than ECL. To fully switch the current to the other side of the current tree, the input voltage difference should be more than 200 mV. Therefore, the input levels are set at Level 1: 0–250 mV and Level 2: $-0.95\,\mathrm{V} - -1.2\,\mathrm{V}$. With CML there is no dynamic power. Power consumption does not change with operation since the total current remains fixed although it is switch from side to side in the logic trees as states change. The two input logic levels establish the required power supply voltage. Therefore the static power load is determined by the current flowing through each logic tree and the number of trees. The total static power consumption of a circuit implemented in CML is quantified by Eq. (1) where N is the number of current trees and I_{ref} is the reference current flowing in a tree.

$$Power = N \times (V_{cc} - V_{ee}) \times I_{\mathrm{ref}}. \tag{1}$$

3. New configurable cell: BC

Different FPGA structures have already been studied [10]; a MUX based FPGA has been shown to have better performance than LUT, NAND and AND-OR based FPGAs. Thus, the reconfigurable logic cell used in the SiGe FPGA uses MUX based configuration. The Xilinx XC6200 FPGA [11] is one of the candidate blueprints of this SiGe FPGA. The Xilinx XC6200 is composed of a large array of simple, configurable cells called BCs. Each one contains a computation unit capable of simultaneously implementing one of a set of logic level functions and

a routing area through which inter-cell communication can take place. This structure is simple, symmetrical and regular, allowing novice users to quickly make efficient use of the resources available. Critics say the Xilinx 6200 family is known for its poor functionality. This is true when compared to some of the modern CMOS FPGAs, however, its open source nature and relatively simple structure makes it a good candidate for high-speed FPGA testing and use in novel applications. For these reasons the authors have precluded other new, more complex FPGA architectures.

3.1. Structure and performance of the configurable cell (basic cell, BC) of the SiGe FPGA

The SiGe configurable cell (Basic Cell) composed of CML MUXs has evolved over several SiGe process generations to optimize performance. The new proposed BC [3], has been designed to tackle the high-power consumption problem that the first generation SiGe Basic Cell had [1], while enhancing the performance and still keeping the same configuration as the original Xilinx 6200. Detailed information of the new SiGe Basic Cell is described below.

The structure of new Basic Cell has three parts; the Input Routing Stage, the Output Routing Stage, and the Configurable Logic Block (CLB). Fig. 3 shows the structure of the new Basic Cell. There are four different kinds of input signals routed to the Input Routing Stage. First is the combinational output (C_x) from its neighbor BCs. Second is the sequential output (Q_x) from four different directions. Third is the bypass outputs of the neighbor cells (x) and the last is the outputs from the neighbor 4×4 array cells ($x4$). The x denotes the direction from which this signal comes. All signals are routed to the two 17:1 MUXs and one 16:1 MUX. After multiplexing, the outputs are routed to the CLB to perform the desired logic function, which is then routed to the neighbor BCs. The Output Routing Stage has four 9:1 MUXs to redirect the inputs of the BC to its neighbors. The Output Routing Stage of the new SiGe BC provides more routing resources compared to the XC6200 BC. This benefit offers more flexibility and functionality to the synthesis

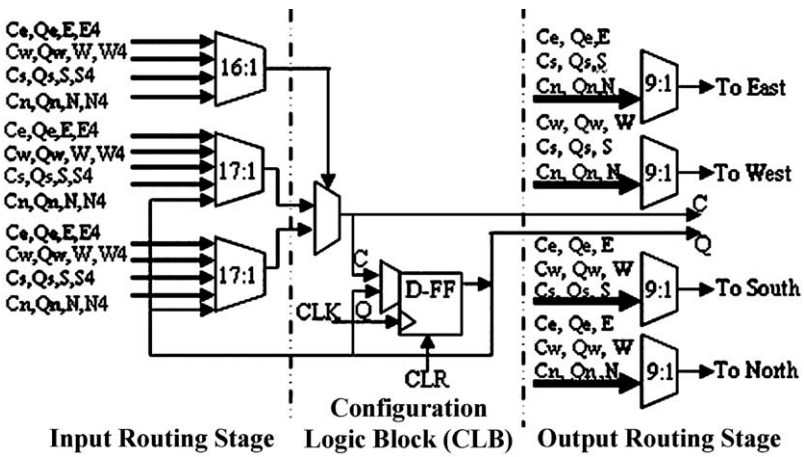

Fig. 3. New BC evolved from Xilinx XC6200 FPGA. C_x and Q_x indicate the combination and sequential outputs from the x directions (Ease, West, South and North).

application tools. The comparison of different generations of BCs is listed in Table 1. It should be noted that the old design (5HP) compared to the new (8HP) BC results in an 83% reduction in propagation delay and 81% reduction in power consumption (8HP power saving case).

To save more power, a power saving scheme has been developed. Table 2 lists three different cases based on the BC's functions with corresponding power usage. Three major functions: combinational logic, sequential logic and redirection signals are simulated and reported [3,12]. The simulation results are listed in Table 2. Each function only uses part of the CML current trees in the BC. The power saving scheme is used to turn off the unused circuits in the BC. Power usages of different cases are listed in Table 3, with the minimum power usage at 14%. By using all power saving techniques, the total power consumption can be further reduced by 99% of the 5HP Basic Cell (239 mW; without a power saving scheme) to the 8HP BC with power saving scheme enabled (1.97 mW; case C). Based on Tables 2 and 3, the total power consumption of a new BC programmed to a specific function can be calculated by Eq. (2) where N is the number of BCs

Table 1
Comparison between the old and new SiGe FPGA design used in this paper

	Process	V_{cc}, V_{ee} (V)	No. of current trees	I_{ref} (mA)	Power consumption per tree (P_{ON})[a] (mW)	T_p (ps)
Old BC [1]	5HP; $f_T = 45$ GHz	0, −3.4	30	0.7	71.4	239
New BC [2]	7HP; $f_T = 120$ GHz	0, −2.8	21	0.8	47.04	100
New BC[b] (high performance case)	8HP; $f_T = 210$ GHz	0, −2.2	21	0.7	32.34	42
New BC[b] Power saving case	8HP; $f_T = 210$ GHz	0, −2.2	21	0.3	13.86	75

[a]A BC is composed of CML trees, each having a fixed current through it that is steered between branches. The power consumption of each basic cell can be calculated by Eq. (1) independent of clock frequency.

[b]The 8HP cases (high-performance case and power saving case) are based on simulations. The difference between the 8HP cases is the high-performance case has its transistors set to the maximum cutoff frequency and the power saving case transistors are set to have the same cutoff frequency as the peak in the 7HP process.

Table 2
Propagation delay and power consumption of the combinational logic, sequential logic and signal bypassed case (AND function)

	Propagation delay T_p (ps)	Power consumption of each function (mW)	No. of enabled current trees	Percent of power used
Combinational logic	49	28	9	43% (9/21)[a]
Sequential logic	109	33.6	12	57% (12/21)[a]
Redirection signal	8	8.4	3	14% (3/21)[a]

[a]The total number of current trees in a basic cell is 21.

Table 3
Power usage of the power saving scheme

Design		No. of Trees	Percent of power used
Case A: Combinational/sequential logic, no redirection		7/9	33%/43%
Case B:	B.1 Comb./sequential, one Redirection	10/12	48%/57%
	B.2 Comb./sequential, two Redirections	13/15	62%/71%
	B.3 Comb./sequential, three Redirections	16/18	76%/86%
	B.4 Comb./sequential, four Redirections	19/21	90%/100%
Case C: Redirection only per direction		3	14%

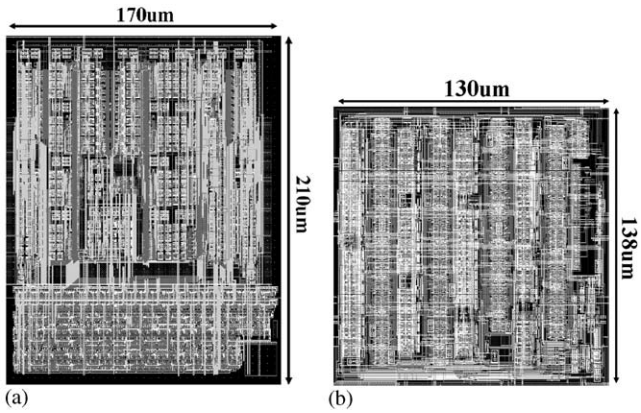

Fig. 4. Layouts of two generations of the BC. Left: 7HP BC dimension $170 \times 210\,\mu m$. Right: 8HP BC dimension $130 \times 138\,\mu m$.

programmed to a specific case and P_{ON} is the fully turned-on power consumption of the new BC (for the 7HP case, the P_{ON} is 47.04 mW).

$$P_{BC} = P_{ON} \times \left(\sum N \times power\ usage\right) \tag{2}$$

The layouts of two different generation BCs are shown in Fig. 4. On the left, the 7HP BC generation has dimensions of $170 \times 210\,\mu m$ and on the right, the 8HP BC has dimensions of $130 \times 138\,\mu m$. The layout has been reduced by 49%.

3.2. Performance of the configurable cell (BC)

Four-stage ring oscillators fabricated by the IBM SiGe 5HP and 7HP Processes have been used to evaluate the speed of the SiGe BCs. Since the SiGe BC is designed to operate in a differential mode, the last stage of each ring oscillator can be inverted just by exchanging its differential outputs. Fig. 5 shows the measurement of the old BC (5HP) four-stage ring oscillator with a period of 240 ps (4.17 GHz). Fig. 6 shows the new BC ring oscillator (7HP) with a period of 100 ps (10 GHz). The operating frequency of each stage of the ring oscillator can be calculated by Eq. (3)

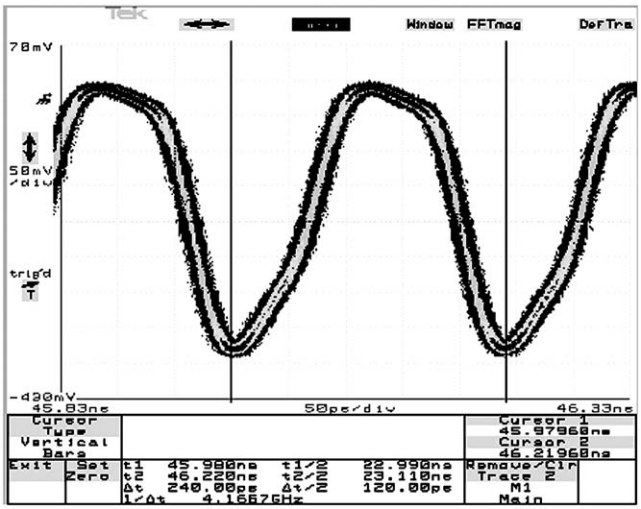

Fig. 5. Measurement of the old SiGe BC [2] four-stage ring oscillator with a period of 240 ps (4.17 GHz).

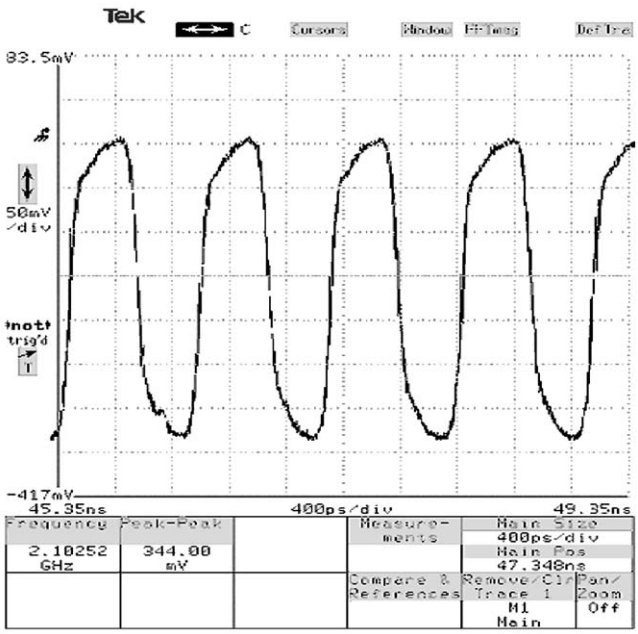

Fig. 6. Measurement of the new SiGe BC [3] four-stage ring oscillator with 1/8th speed period of 800 ps (10 GHz).

where N is the number of stages and T is the period of the ring oscillator.

$$f = \frac{1}{2NT} \tag{3}$$

Based on this equation, the new Basic Cell can operate up to 10 GHz—double the maximum speed of the older 5HP design. Thus, by using a more advanced process, the performance of the BC is proportionally increased.

4. 4:1 multiplexer (4:1 MUX), 1:4 demultiplexer (1:4 DEMUX) and pipelined adder implemented in the SiGe FPGA

Fig. 7 shows an application example based on the proposed high-speed reconfigurable system for data acquisition. A VCO generates a 16–24 GHz clock for use with a 40 GHz interleaved ADC. The outputs of the four ADC channels are interleaved by the SiGe FPGA (configured as MUXs) to reduce the operating frequency of 10 GHz to 500 MHz so that lower power CMOS FPGAs can process the data. The outputs of the CMOS FPGA is then routed back to the SiGe FPGA to recombine the data to a high speed analog signal using a high-speed DAC.

For this high-speed reconfigurable data acquisition system, an ADC with 10 GS/s has been proposed [13]. The SiGe FPGA programmed as a 4:1 MUX and 1:4 DEMUX has been evaluated to ensure it interleaves and de-interleaves signals correctly. A smaller DSP application with the relative size of the SiGe FPGA can be implemented too.

Many high-speed MUX and DEMUX designs have been developed based on the different processes, with the latest reported design having a data transfer rate up to 40 GHz [8,14,15]. However, no reconfigurable gigahertz MUX and DEMUX implemented in an FPGA has been reported. By implementing them, the performance of the SiGe FPGA in the high-speed reconfigurable data acquisition system can be evaluated and compared to conventional CMOS FPGAs. The FPGA MUX-DEMUX cannot reach the speeds of the specialized but very expensive MUX-DEMUX ASICs, such as SERDES, since it is limited by the BC unit, thus specialized design techniques such as Cherry-Hooper amplifiers and peaking inductors cannot be used. However, when used as a basis for comparison, it can be shown that the performance of the SiGe FPGA far exceeds that of the CMOS FPGA.

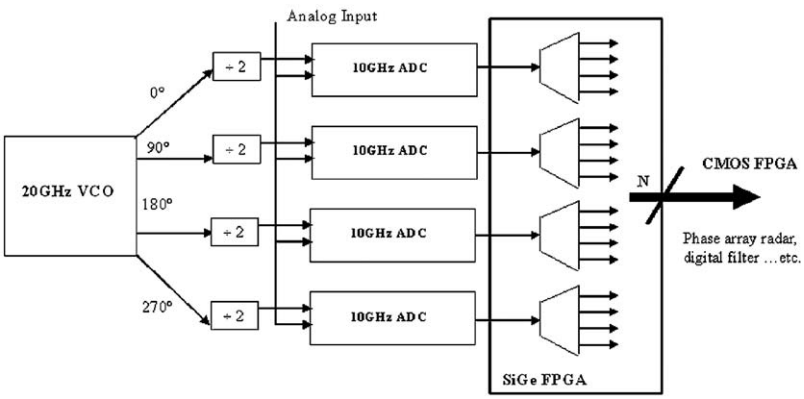

Fig. 7. Proposed data acquisition system with the SiGe FPGA between the high-speed front-end and CMOS FPGA.

The VCO [16], with a target range between 7–13 GHz and center frequency at 10 GHz, is used as a test input for the data acquisition system created with the SiGe FPGA programmed as a 4:1 MUX and 1:4 DEMUX. From simulations, the frequency range of the VCO can be set between 9.2–16.5 GHz. The measured frequency is around 8 – 14 GHz with the input voltage range at −0.7 to −1.2 V.

4.1. 4:1 MUX implementation

Fig. 8 shows the routing schematic of a 4:1 MUX with a tree architecture, where the building elements are a recursive series of 2:1 MUX modules shown as the dashed block. It takes four channel data streams (CH1–4) with a half rate input clock to create the final 4:1 MUX outputs in this case. From the previous sections, the input data frequency that the SiGe FPGA can deal with is up to 10 GHz. With this the goal of the 4:1 MUX is generating a 10 Gbps multiplexed output data stream. The inputs of all data streams (CH1–CH4) are generated by a Pseudo Random Bit

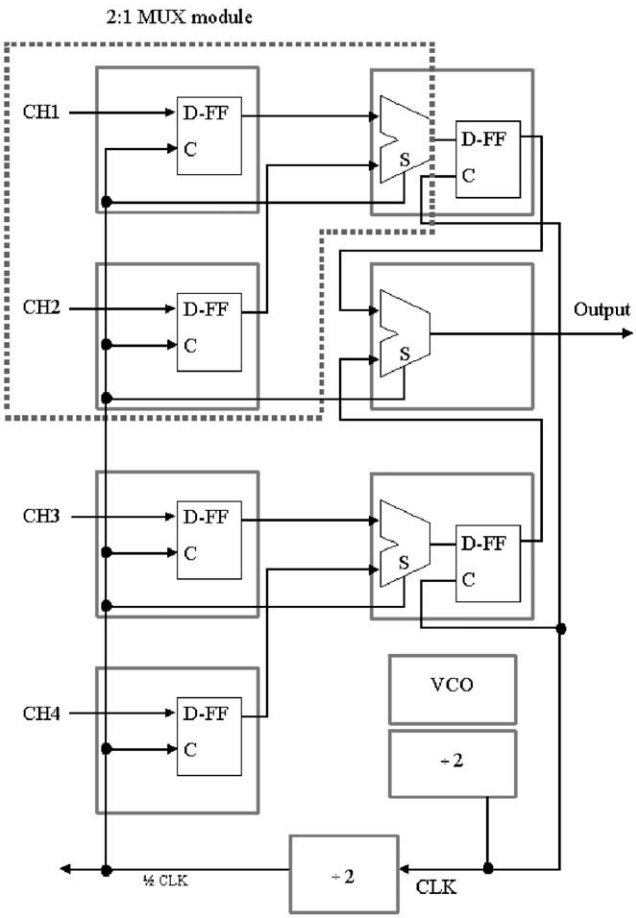

Fig. 8. Schematic of the 4:1 MUX implemented in the SiGe FPGA.

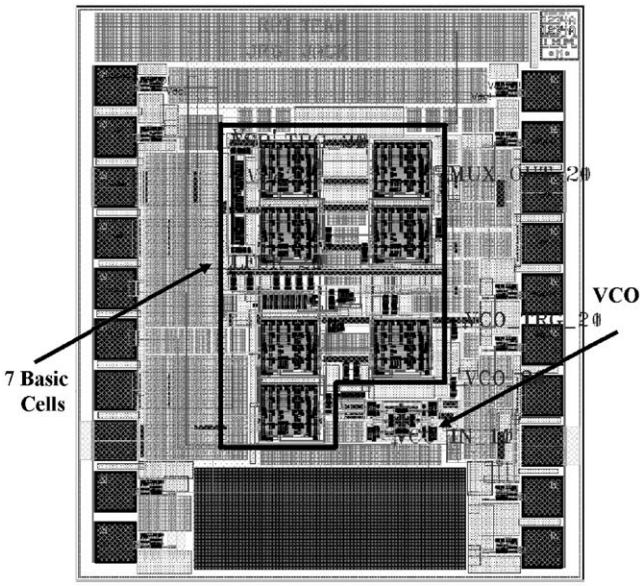

Fig. 9. Layout of the small SiGe FPGA implemented with the 4:1 MUX.

Sequence (PRBS) with a 2.5 GHz clock source generated by the VCO. In the 4:1 MUX, the clock signals (CLK) are two times faster than the clock (1/2 CLK) applied to the previous modules. Both clocks are also generated by the VCO. The first two BCs in the 2:1 MUX module are configured to perform D-FF functions that align the timing of the data streams to the slower clocks (1/2 CLK). The right side BC is configured to be a multiplexer and a D-FF to select different data streams and align to the next stage timing (CLK). When the select signal S is high, the multiplexer selects the CH1 data stream. When S goes low, the multiplexer selects the CH2 data stream. In order to align the timing of the multiplexed data streams, the clock connected to the top of the 2:1 MUX Module is inverted. Thus, the phase of the output data stream can be offset by 180°. Then both outputs of the 2:1 MUX modules are passed to the next module.

A small SiGe FPGA is configured to be the 4:1 MUX. Seven BC cells are used to implement this 4:1 MUX. Fig. 9 shows the layout of the SiGe FPGA implemented to a 4:1 MUX.

4.2. 1:4 DEMUX implementation

Fig. 10 shows the block diagram of the 1:4 DEMUX implemented by 8 BCs. It receives a full-rate differential data stream and outputs four parallel data streams. Like the 4:1 MUX, the 1:4 DEMUX also uses a tree-architecture with a recursive series of 1:2 DEMUX stages in which every stage uses latches to demultiplex and align the data streams with the clocks generated by the VCO. The input high-speed data stream (10 Gbps) is latched by the first BC cell in the first DEMUX stage to align with the CLK (10 GHz). Using the rising and falling edges of the clock (CLK), the input is demultiplexed into two different data streams. Then the separate streams are passed to the

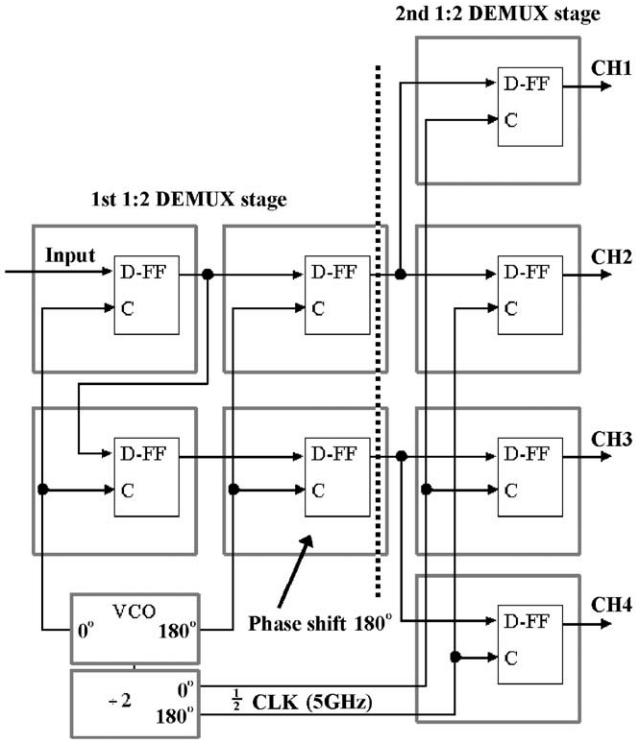

Fig. 10. Schematic of the 1:4 DEMUX implemented by the SiGe FPGA.

second multiplexer stage to separate them again into four different output data streams. Fig. 11 shows the layout of the small SiGe FPGA programmed as a 1:4 DEMUX.

5. Performance of the 4:1 MUX and 1:4 DEMUX

The simulation results of the 4:1 MUX are shown in Fig. 12. The input and output data stream patterns are listed below it. The input data streams are generated by a PRBS with a 2.5 GHz clock provided by the VCO described previously. The output transmission rate is at 10 Gbps. Fig. 13 shows the eye diagram of the SiGe 4:1 MUX. Compared to the same eye-diagram of the same circuit implemented in a CMOS FPGA, the SiGe MUX's eye opening is wider than its CMOS competitors.

Regarding the power consumption of the 4:1 MUX, since the power saving scheme is used, the total power has to be calculated by the real implementation layout. From the layout, there are 5 and 2 BCs configured to Cases A and B.1 respectively. Therefore, the total power consumption of the implemented 4:1 MUX based on Eq. (2) is 146.3 mW.

$$P_{4:1\mathrm{MUX}} = 47.04\,\mathrm{mW} \times (5 \times 43\% + 2 \times 48\%) = 146.3\,\mathrm{mW}. \tag{4}$$

Fig. 14 shows the simulated output waveforms of the 1:4 DEMUX. The input and output data streams are also shown below it. It has 6 and 2 BCs configured as Cases A and B.1 respectively with a total power consumption of 166.52 mW. The output pad power consumption is

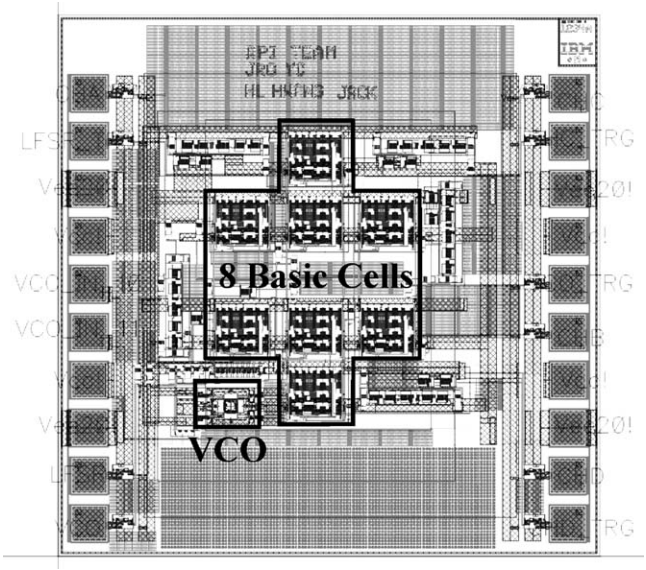

Fig. 11. Layout of 1:4 DEMUX implemented by the SiGe FPGA (8 BCs).

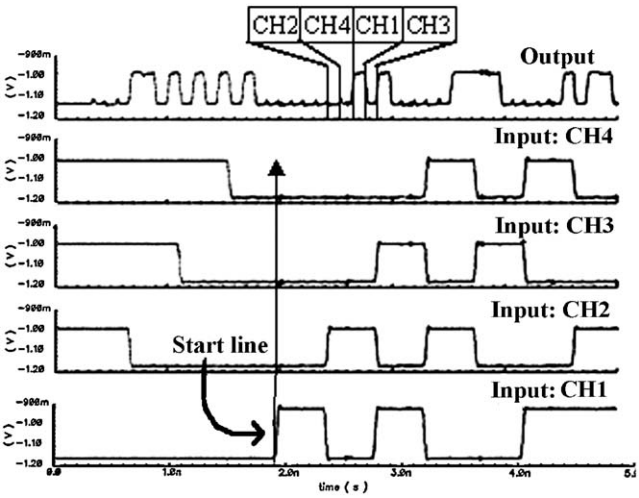

Fig. 12. Simulation result of the 4:1 MUX. Inputs: CH_A: 1010011, CH_B: 0010100, CH_C: 0101001 and CH_D: 0001010. Output: 0010-1000-0011-1100-0001-0110.

28 mW (1 output with a reference current equal to 10 mA). The total estimated power consumed is 195.5 mW.

$$P_{1:4\mathrm{DEMUX}} = 47.04\,\mathrm{mW} \times (6 \times 43\% + 2 \times 48\%) = 166.52\,\mathrm{mW}. \tag{5}$$

The 4:1 MUX and 1:4 DEMUX have also been implemented on a Xilinx Virtex protoboard [17]. The Virtex family has a newer structure to provide better performance and more I/O standards to communicate with other circuits. Xilinx Foundation 2.1 is used to implement the 4:1

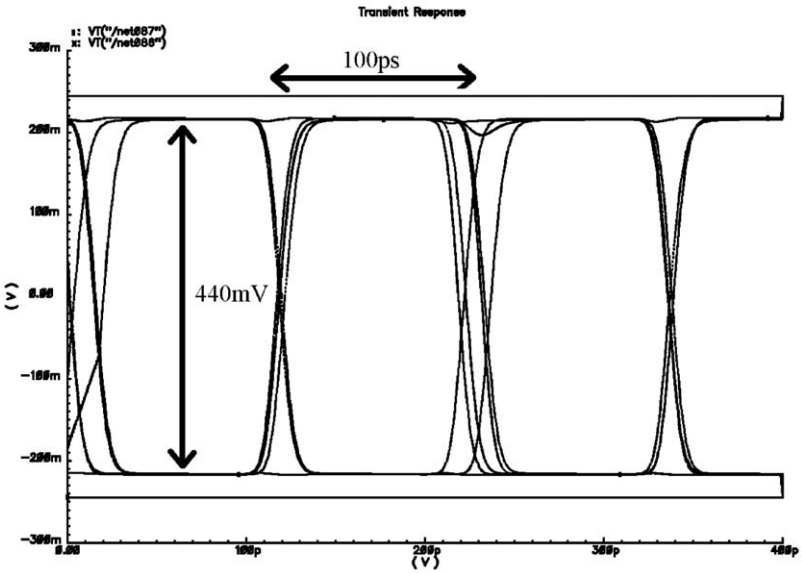

Fig. 13. 4:1 MUX simulated output eye-diagram.

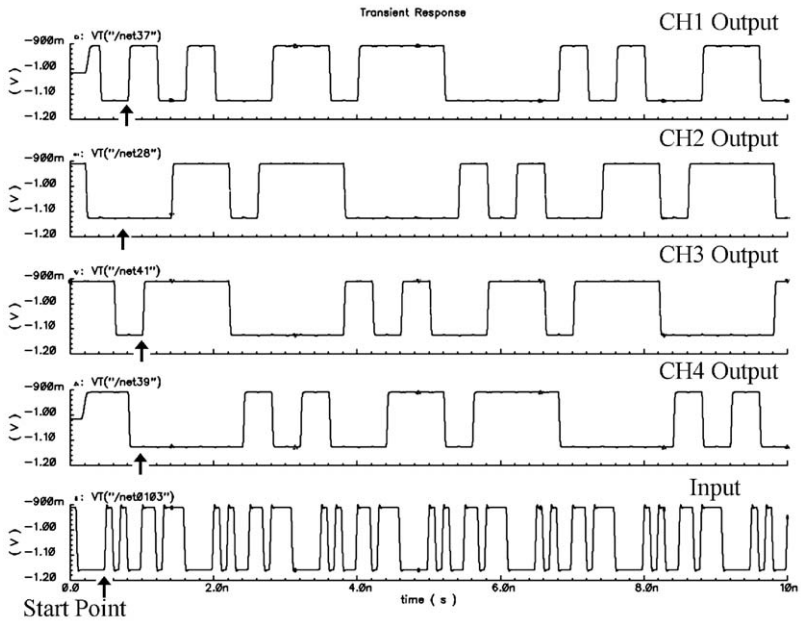

Fig. 14. The simulation result of the 1:4 DEMUX. DEMUX-input: 1010-0110-1110-0001-0100-1101-1100. Outputs: CH1: 1 0 1 0 0 1 1; CH2: 0 1 1 0 1 1 1; CH3: 1 1 1 0 0 0 0; CH4:0 0 0 1 0 1 0.

MUX and 1:4 DEMUX on the Xilinx Virtex protoboard. The 4:1 MUX's fastest clock period is set to 200 MHz. However, measurement results only yielded support to 183 MHz. With the 1:4 DEMUX, the Virtex showed correct operation up to 182 MHz.

Table 4
Comparison of the performance of the SiGe and CMOS FPGAs

	Tx rate	Power consumption (mW)	No. of CLB used
4:1 MUX (SiGe FPGA)	10 GBps	146.3	7
4:1 DEMUX (Xilinx Virtex)	183 MHz	53	7
1:4 DEMUX (SiGe FPGA)	2.5 Gbps (Input: 10 Gbps)	166.52	8
1:4 DEMUX (Xilinx Virtex)	45.5 MHz (Input: 182 MHz)	79	8

To calculate the power consumption of a design implemented by the Xilinx FPGA, Xilinx provides a web-based work sheet (V1.5) to estimate this parameter [18]. Its power estimator is based on the design's resource usage, toggle rates and other factors. By using this work sheet, the power consumption of the implementations can be calculated and compared to the SiGe FPGA. Based on the data from [18], the 4:1 MUX has a power consumption of 53 mW and the 1:4 DEMUX has a power consumption of 79 mW. From these results, 4:1 MUX implemented by the SiGe FPGA is 2.76 × and the 1:4 DEMUX is 2.1 × larger than the CMOS FPGA implementation results. These values are summarized in Table 4.

6. Conclusion and future work

The newly proposed SiGe BC has been proven to run up to 10 GHz. After several generation developments, its propagation delay, power consumption and the layout size have been greatly reduced to make larger scale SiGe FPGAs possible. With the proposed high-speed reconfigurable data acquisition system, the SiGe FPGA is used as the interleaving and de-interleaving stage. To demonstration that the proposed system is feasible, the SiGe FPGA will be configured as a MUX and DEMUX to interleave the GHz signals to several lower-frequency channels into the CMOS FPGA. Two test circuits are being fabricated to assess the performance of the SiGe FPGAs implementing the 4:1 MUX and 1:4 DEMUX. Simulations show that they correctly operate at a 10 GHz clock frequency. A comparison between the SiGe FPGA and CMOS FPGA has also been done. With several power saving techniques that have been developed, the SiGe FPGA implemented with the 4:1 MUX and 1:4 DEMUX have only 2.76 and 2.11 times the power consumption compared to their CMOS counterparts.

After demonstrating the feasibility of the SiGe FPGA in the reconfigurable data acquisition system, the future work will be to integrate the SiGe and CMOS FPGA with a high-speed ADC/DAC, allowing it to be used on gigahertz frequency signals.

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