A Novel Multi-Speed, Power Saving Architecture for SiGe HBT FPGA

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Abstract

The availability of SiGe HBT devices has opened a door for Gigahertz FPGAs. However, the large device power consumption limits its scale. In order to solve this problem, a Multiple-Speed Current Mode Logic design has been developed to provide variable power (and speed) settings. The performance of the Multiple-Speed Current Mode Logic architecture at the optimum setting exhibits similar performance to conventional Current Mode Logic designs. The Multi-Speed FPGA has been developed based on this new design. The economic power setting (lower speed setting) does not degrade its performance substantially. With this power saving technique the Multiple-Speed FPGA, therefore, can be scaled up in the future.

Key words: SiGe, HBT, CML, Power Saving architecture, FPGA.

1. Introduction

The Field Programmable Gate Array (FPGA) is a configurable circuit consisting of logic blocks surrounded by a programmable routing structure. The structure is shown in Figure 1. The input signals (A, B and C) are passed through the I/O cells on three different sides of the routing cells, and then steered to a configured logic cell. The routing cells and logic cells are programmed by memory whose data is generated by CAD software to perform the desired functions. Currently, the versatility of the FPGA has made them useful for applications such as network routers. However, the relatively low operating frequency of current commercial FPGAs limits their use in high frequency applications.

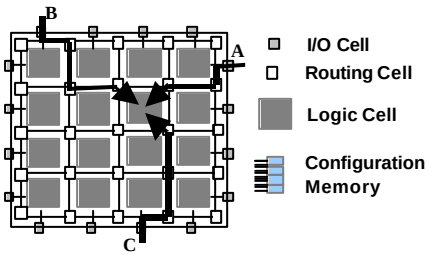

Figure 1. The structure of an FPGA

A high-speed FPGA has been demonstrated using the Current Mode Logic (CML) [1], [2]. It has established the feasibility of multi gigahertz FPGA.

The Xilinx 6200 FPGA has been chosen for the blueprint of the prototype gigahertz FPGA. It was selected because the bit programming information has been released to the public and its architecture, consisting of multiplexers (MUXs) and flip-flops (FFs), is easily converted to Current Mode Logic (CML). Figure 2 shows the basic cell with Function Unit (Configurable Logic Block) of the Xilinx 6200 FPGA [3]. Two inputs are routed from x1, x2 and x3 into the CLB. By properly setting the control bits, the CLB can be configured to the desired logic function. Power consumption has traditionally been a serious problem in CML design, due to the high static current flow. We have developed a multilevel architecture to reduce the overall power consumption for the SiGe CML FPGA.

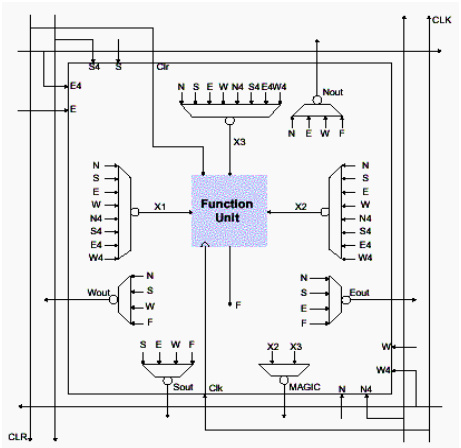

Figure 2. The basic cell with Function Unit (Configurable Logic Block) of the Xilinx 6200 FPGA.

Section 2 describes the Silicon Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) and compares

some similar processes. Section 3 shows the basic characteristics of CML such as propagation delay, rise time and fall time. Section 4 and 5 demonstrate the Multi-Speed CML and compare its performance to conventional CML. Section 6 shows the Multi-Speed FPGA logic verification, and performance. A one-bit adder is presented to verify the logic performance of the circuitry. Section 7 describes the fabricated chip to validate the simulation results of previous sections. Finally, the results are summarized and conclusions drawn for future directions.

2. IBM 120 GHz SiGe Process

The IBM SiGe BiCMOS process has evolved over several generations, in which the HBT's cutoff frequency approaches 120 GHz (for 7HP) and is still increasing; a 210 GHz process (8HP) is under development. Figure 3 shows the cutoff frequency of the 0.5 & 0.25 µm processes: 43 GHz. The 0.18 µm reaches 124 GHz.

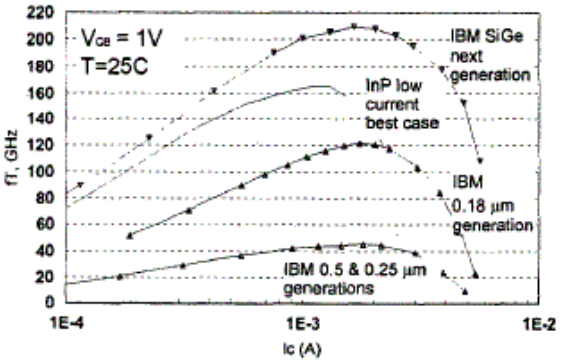

Figure 3. Cutoff frequencies of several SiGe Technologies and InP

From figure 3, it is observed that the cutoff frequency of the next generation IBM SiGe process is higher than InP processes. Thus, the HBT high frequency performance has caught up with traditional III-V devices such as GaAs and InP. The excellent high frequency performance of the 120 GHz devices has been demonstrated most recently [4]. With its outstanding high frequency characteristics, digital circuits can be created to operate up to 40 GHz. Figure 3 shows that the collector current varies logarithmically with the operating speed (f_T) of the device. For example, in the IBM SiGe 0.18µm generation, the peak collector current is 0.9 mA at its maximum frequency (124 GHz). Half that current has yields a cutoff frequency at 95 GHz. We may take advantage of this to create a circuit with lower power consumption and experience little performance degradation.

3. Current Mode Logic (CML)

CML is the second generation of Emitter Coupled Logic (ECL). Like ECL, it is a differential logic design methodology that focuses on steering currents instead of switching on and off. It has many similarities to ECL design, such as preventing the transistor from saturating and wide use of emitter coupled differential pairs. The advantages that make CML unique are that it doesn't require emitter followers at the gate outputs and it can be biased at lower current levels without appreciably degrading its speed. Overall, less power is consumed with CML than ECL.

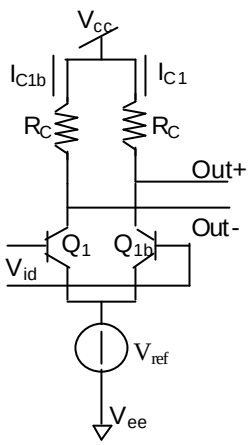

Figure 4. A conventional CML Buffer

Figure4 shows a CML buffer. A reference current is provided at the bottom of the current tree. By properly steering the current (I_{ref}) flow through the switching transistors (Q_1 and Q_{1b}) and the collector resistors; the desired output voltage is achieved.

4. Multi-Speed (MS) CML

Though CML has many advantages over other types of digital logic, it has a significant power consumption problem. Since there is always current flowing in the logic tree, the static power consumption occupies a significant percentage of the power that the circuit consumes. To CMOS, it has only dynamic power consumption, consuming power while the transistor is switching. If the CML reference current can be reduced, the static power consumption can be lowered. However, reducing the reference will also sacrifice the speed of the circuit. With variable reference current, a CML gate

can be adjusted from a high-speed (with higher power) to lower speed (with more power saved).

Figure 5 shows the Multi-Speed CML with N Multi-Speed Load Modules (MS-LMs). Including a pair of diodes and resistors to replace the resistor load of the CML buffer on the top allows multiple reference currents to be used while maintaining a consistent voltage drop. If V_{on-1} is high and V_{on-2} ~V_{on-N} are low, the current flows through V_{on-1}, D_{1-1}, (or D_{2-1}) and R_1 to lowest voltage node. To prevent the current from flowing to other modules, the diodes are added. There are N MS-LMs in the MS-CML buffer and a variable current source (I_{ref}) to provide different reference currents to different modules. The output voltage should be kept to at least 200 mV to insure a full switch of current from one side of the tree to the other. Vout can be calculated in the equations below (Eq -1):

V_{on-1} = High; others = Low:

$$? \, Vout \, ? \, I_{ref\,(Von?1?\,high)} \, ? \, R_{1?1}$$

V_{on-2} = High; others = Low:

$$? \, Vout \, ? \, I_{ref(Von?\,2?high)} \, ? \, (R_{1?1} \, ? \, R_{1?2})$$

$$\vdots$$

V_{on-N} = High; others= Low.

$$? \, Vout \, ? \, I_{ref(Von?\,N\,?high)} \, ? \, (R_{1?1} \, ? \, R_{1?2} \, ? \, ???? \, R_{1?\,N})$$

-Equation 1

The remainder of this paper discusses a 2 speed MS-CML circuit, with reference currents of 1mA (peak f_T current) and 0.5mA (one half peak f_T current), referred to as high speed and economic power savings mode, respectively. Both settings are compared to a traditional CML circuit in section 5.

5. Performance comparison of conventional CML and Multi-Speed CML buffers

The buffer test circuit diagram is shown in Figure 6. The test pattern is passed through a 3-stage buffer to the test circuits (CML buffer and MS-CML buffers) that are loaded with three single stage CML buffers. Of the three buffers, two are identical (MS- CML buffers) but are programmed for two different modes. Circuit performance is evaluated based on two criteria: propagation delay and rise/fall time.

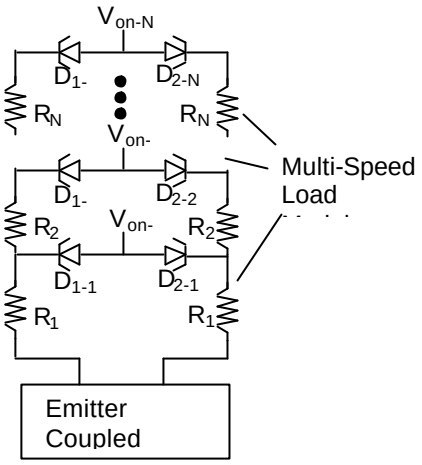

Figure 5. MS- CML buffer with N speed modules

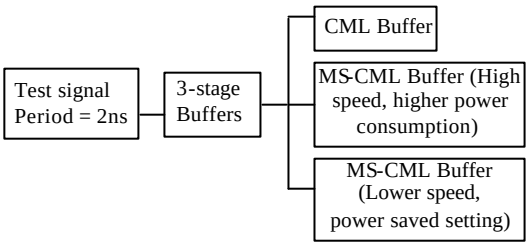

Figure 6. Buffer test circuit for comparing the performance of buffers

5.1. Propagation delay comparisons (T_P)

From Figure 7, the conventional CML buffer and high-speed mode MS-CML buffer are observed to have similar T_P. They are 9.72 ps and 10.18 ps. This demonstrates that T_P doesn't degrade much after adding two multi-speed load modules (in high speed mode). The economic power mode MS-CML buffer has a larger T_P than previous two circuits as expected.

It is 15.85 ps, about 63% and 56% more than the conventional CML and high-speed mode cases.

	Conventional CML	Multi-Speed CML buffer (High speed, power consuming mode)	Multi-Speed CML buffer (Lower speed power economic mode)
T_P	9.72 ps	10.18 ps	15.85 ps
T_r	31.93 ps	49.98 ps	71.71 ps
T_f	29.46 ps	21.91 ps	39.11 ps
Vout	220.1 mV	217.3 mV	205.8 mV
Frequency of the ring oscillator	66.67 GHz (150 ps)	64.93 GHz (154 ps)	49.01 GHz (204 ps)

Table 1. Simulation result of the conventional CML buffer and the Multi-Speed CML buffer.

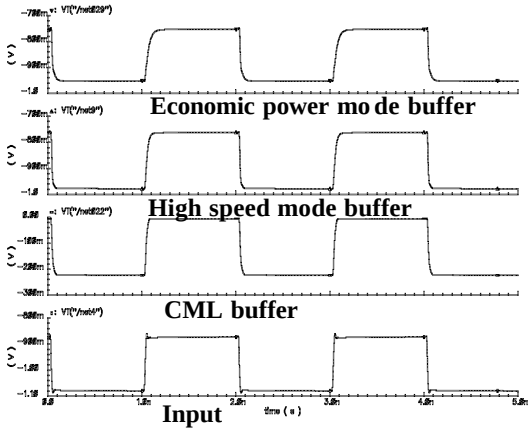

Figure 7. Simulation of the buffer test circuit. (From top to bottom: economic mode and high speed mode MS-buffers, CML buffer and input signal

5.2. Rise Time (T_r) and Fall Time (T_f)

The T_r of the conventional CML buffer and both the high speed and economic power mode of the MS-buffer are about 32 ps, 50 ps and 72 ps. The influence of adding those modules to replace the resistors is that the rise time is degraded. Fortunately, when the rising edge of the signal is 80% of the voltage swing, the T_r is 47.53 ps. Then it slowly reaches 90% (in additional 24.18 ps). The powers saving modules also influence the T_f of these buffers. But it is worth pointing out that the fall time of the MS-CML buffer in high-speed mode is lower than the CML buffer; a positive effect.

5.3.Ring Oscillator Tests

The ring oscillator circuit consists of 10 single stage buffers. Three ring oscillators (CML buffers, high speed and power economic mode MS-buffers) are tested. The CML, high-speed MS-CML, and power-savings MS-CML ring oscillators operated at frequencies of 66.67 GHz, 64.93 GHz and 48.96GHz respectively. The data is summarized in Table 1.

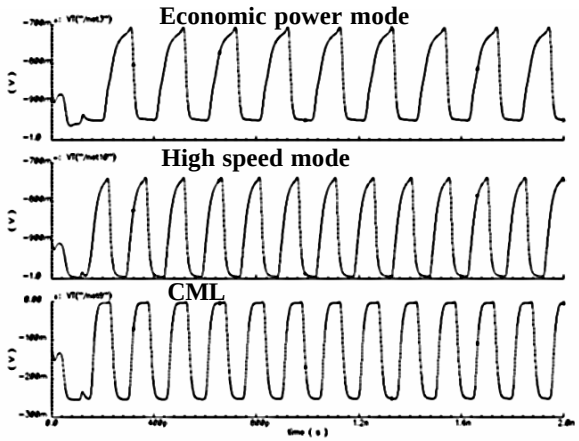

Figure 8. Simulated waveform of ring oscillators (From top to bottom: MS-buffer ring oscillator with power economic mode and with high speed mode and CML buffer ring oscillator)

6. The application of the Multi-speed CML circuit to the FPGA

In the first gigahertz FPGA design [1] and [2], the power consumption was very large. Therefore, a new design has been developed using the MS-CML methodology. Depending on the clock frequency of a design, the new FPGA can be programmed to specifically operate in economic power mode when possible to reduce the static power that is consumed.

6.1. Configurable Logic Block (CLB) characteristics, logic validation and application

Figure 9 shows the schematic of the Configurable Logic Block of Xilinx 6200. The CLB is composed of five 2 to 1 multiplexers (2:1 MUXs) and one D-flip flop. For testing, three CLBs have been created. CLB-1 is composed of the convent ional CML and CLB-2 and -3 are composed of the MS-CML programmed for high-speed mode and economic power mode. Compare to the original CLB in the Xilinx 6200, this CLB is the combinational logic part.

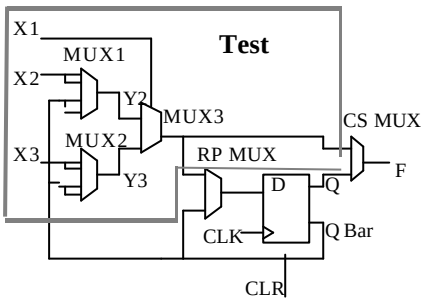

Figure 9. The CLB schematic for logic verification.

Figure 10 shows the AND simulation results. The propagation delay of the CLB-1 (CML, 17.79 ps) is faster than CLB-2 (high speed mode, 19.87 ps) and -3 (economic power mode, 34.28 ps). The smoother rise time of the CLB-2 and -3 are expected as previous paragraph mentioned.

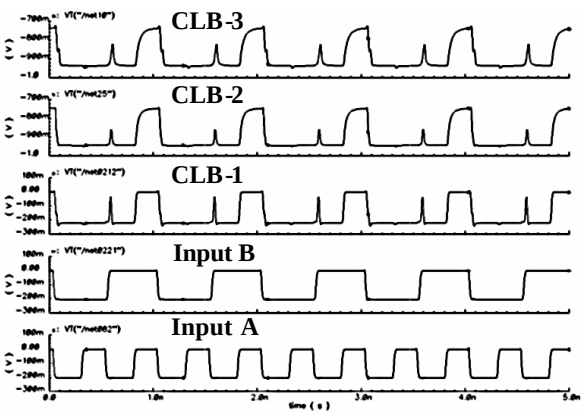

Figure 10. Simulation result for the AND logic. (From the top to bottom: CLB-3 output, CLB-2 output, CLB-1 output, input B and input A)

Figures 11 and 12 show the simulated waveforms of the CLB-1, CLB-2 and CLB-3 four stage ring oscillators. The T_P of the CLB-1 ring oscillator is 162.61 ps (24.61 GHz). The T_P of the CLB-2 ring oscillator is 163.03 ps (24.53 GHz) and the T_P of the CLB-3 ring oscillator is 293.4 ps (13.63 GHz).

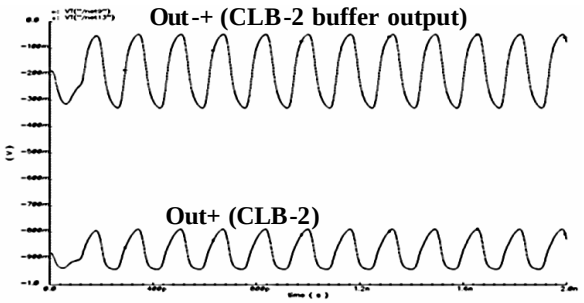

Figure 11. Simulated waveform of the ring oscillator composed of the CLB-2 and the ring oscillator outputs.

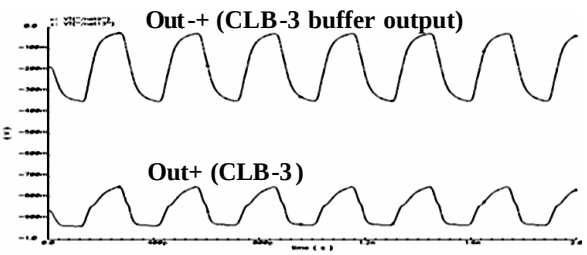

Figure 12. Simulated waveform of the ring oscillator composed of the CLB-3 and the ring oscillator outputs.

Figure 13 shows a one-bit full adder that requires three logic gates to synthesize. The three CLBs are programmed as XOR and 2:1 MUX logic. The adder's CLB is replaced by CLB-1, CLB-2 and CLB-3 and simulated to understand the performance of MS-CML with several CLBs connected. The sum of the CLB-1, CLB-2 and CLB-3 adders are shown in Figure 14 with T_P of 35.6 ps, 33.26 ps and 57.23 ps respectively

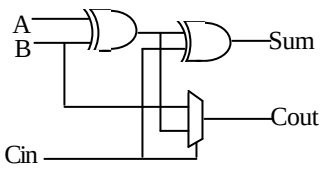

Figure 13. Block diagram of a one-bit adder

	CLB-1	CLB-2	CLB-3
T_P of the CLB	17.79 ps	19.87 ps	34.28 ps
Ring oscillator frequency	24.61 GHz (Reference [1])	24.53 GHz (163.025 ps)	13.63 GHz (293.41 ps)
Power consumption per CLB	14 mW	14 mW full power	7 mW half power
T_P of the one bit adder	35.6 ps	33.2 ps	57.2 ps

Table 2. CLB performance and power consumption

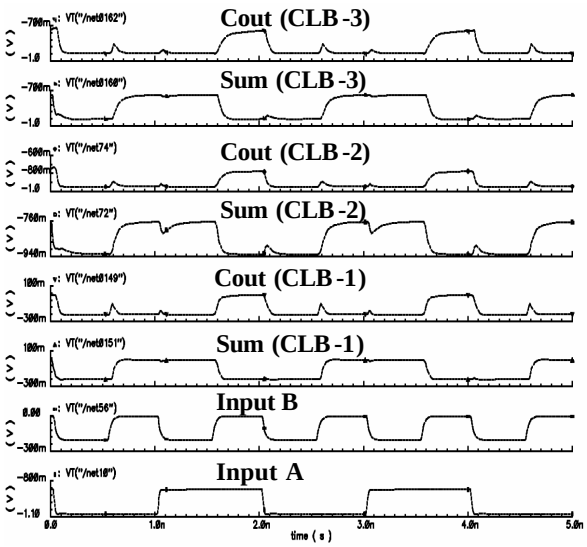

Figure 14. Simulation results of the one-bit adders (From top to bottom: Cout and Sum of CLB-3 adder Cout and Sum of CLB-2 adder Cout and Sum of CLB-1 adder and input B, input A.)

6.2. Power Consumption of CLBs

Since the purpose for designing multi-Speed CML is to find a way to reduce the power consumption of an FPGA, power calculations are necessary. CML and MS-CML in high-speed mode consume the same amount of power (3.5 mW) for each current tree. The MS-CML in economic power mode can save half of the power, reducing the consumption to 1.75 mW. From the above CLB structure, we can see the number of current tree needed is 4 for the test part.

Table 2 summarizes the performance and power consumption of the CML CLB, and the MS-CML in both power modes. The implemented test structure shown in Figure 9 shows that four current trees are needed to implement a CLB.

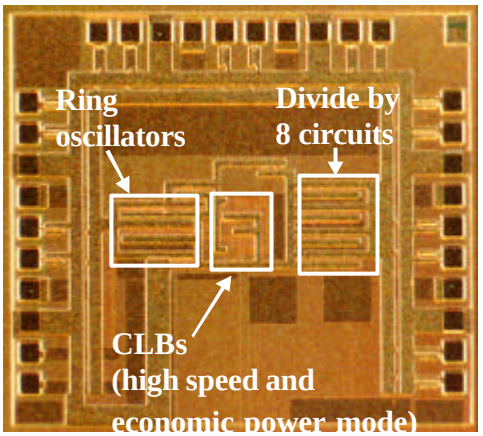

Figure 15. Micrograph of the test chip

7. Test chip

A test chip was fabricated to verify the simulated data. Figure 23 shows the layout of the test chip. It consists of three 10 stage ring oscillators (CML, MS-CML in high-speed mode and in economic power mode) to test the performance of both modes of the MS-CML. For the CLB test, a 10-stage CML ring oscillator was used to generate the input signals for the CLB in order to validate the logic and simulated performance results. For measurement, the output frequency of the ring oscillators and CLB test part is divided by 8. The photograph of the test chip is shown in Figure 15. The chip has just returned from fabrication and thus we are unable to provide actual chip results at this time.

8. Summary

Multi-Speed CML has been developed as a method for conserving power through the use of selectable operating speeds for multiple power consumption levels. For the FPGA, MS-CML provides a means for operating only critical portions of the IC at full speed (full power) while maintaining optimum speed. This provides a way to reduce the power consumption

MS-CML has been simulated by three major tests. First, the ring oscillator composed of buffers show what frequencies can be achieved. Second, the Multi-Speed CLB has been constructed and tested. It shows similar performance to the conventional CLB described in [1]. Third, three CLB blocks are constructed with each one programmed to a specific logic function. The performance of a CLB-2 adder has similar characteristics to the CLB-1 adder, but the trade-off of adding the Multi-Speed modules is an increased rise time.

9. Conclusion

With the help of the SiGe process and high speed circuit design techniques, the operating speeds of CML SiGe FPGAs has reached gigahertz levels—much greater than the maximum speeds of commercial CMOS FPGAs at this time. However, the high power consumption associated with CML logic has limited the scale of CML FPGAs. With the newly designed Multi-Speed CML, the power consumption can be reduced significantly by programming portions of the FPGA to operate in the economic power mode using a smaller reference current, without sacrificing too much speed. By properly utilizing the MS-CML design, a significant power savings can be achieved, paving the way for larger scale gigahertz CML FPGAs.

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