"SiGe HBT BiCMOS Field Programmable Gate Arrays for Agile Mixed Signal Applications"

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Abstract

CMOS Field Programmable Gate Arrays or FPGA's are flexible hardware circuits, which can be used to implement a wide variety of digital functions, and offer total re-configurability. However, at least in current CMOS generation, system clock rates are typically around 100-200MHz. There are, for example, no CMOS FPGA's operating in K-band. Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBT's) are devices that offer significantly higher speed. By implementing FPGA's using SiGe HBT circuits a new capability for much higher speed may become possible.

1. INTRODUCTION

Field Programmable Gate Arrays are integrated circuits that can be reconfigured to implement different digital hardware functions, making them excellent candidates for applications requiring fault tolerance and mission agility. The FPGA consists of 2-dimensional array of universal logic modules (ULM's) or Component Logic Blocks (CLB's) that can be configured to realize units in large family of digital logic elements [1,2]. However, currently FPGA's are implemented in 0.13 micron CMOS and limited to implementing systems at 100-200 MHz. At this time there are currently no FPGA's that operate at the speed of Microprocessor Clock rates, much less at X-band, or K-band. Systems that require data acquisition, signal generation or signal processing at millimeter frequencies must operate at least partially in that frequency range.

1.1 Silicon Germanium Heterojunction Bipolar Technology

SiGe HBT device technology was pioneered at IBM originally for advanced computer applications. However, it has found its greatest use thus far for wireless applications [3]. FPGA's are currently implemented in 0.13 micron CMOS technology where device maximum frequency, f_T, is about 67 GHz. Silicon Germanium Heterojunction Bipolar Transistors (SiGe HBT's) at the 0.13 micron technology node (termed 8HP) offer f_T=210GHz. In addition to this outstanding f_T, the minimum-sized bipolar device has a much lower on-resistance (~100 ohms) compared to the minimum-sized FET (~ 9,000 ohms), giving it an advantage in driving wire both on the chip and off. Flip-flops utilizing this HBT can toggle at 80 GHz. While evolution of both FET and HBT device performance is difficult to predict, at this point in time it is of interest to know how much of an improvement SiGe HBT devices can bring to FPGA circuits. SiGe HBT technology brings some of the speed of III-V devices to silicon processing and even permits co-integration of the HBT with CMOS.

1.2 Choice of the Initial SiGe-HBT BiCMOS-FPGA Architecture

In order to achieve an early demonstration of the possibilities for high-speed FPGA circuits, the Xilinx XC 6200 FPGA was chosen for emulation in SiGe. Emulation of the XC 6200 provides access to any configurations that have been developed for the part in the past. The programmable bit stream definitions that configure the XC 6200 are in the public domain. In addition, a legacy of Computer Aided Design tools exists to generate other configuration bits from user specified designs. This facilitates a rapid exploration and evaluation of the merits of SiGe in this application [4]. However, longer term if this effort is successful other FPGA architectures may offer advantages relative to the XC 6200. The XC 6200 uses a multiplexer based CLB, which makes it especially appropriate for interleaving or de-interleaving data streams with variable numbers of interleaving channels and variable word size. This might make the XC 6200 especially important for such applications as agile poly-phase or block filtering, for example.

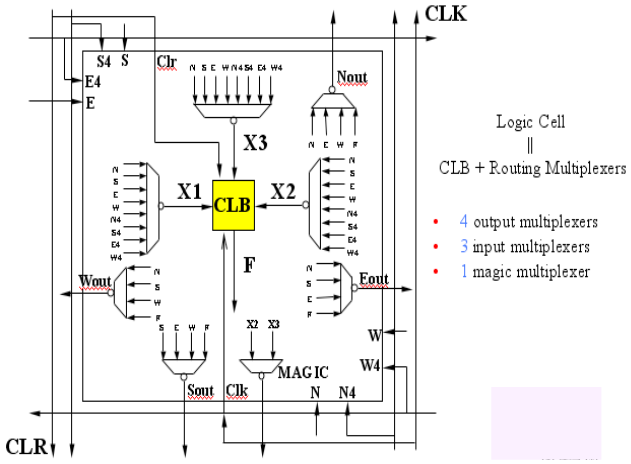

Figure 1. The XC 6200 "tile" or Logic Cell showing CLB core and signal-multiplexers for NESW routing.

The FPGA consists of a tiled array of logic cells that contain the basic CLB, and its associated signal routing multiplexers, as shown in Figure 1. The use of multiplexer circuits to route signals does impose the delay of these multiplexers on signal

propagation. However, they also permit wider bandwidth than possible with the pass transistor switches that are used in most CMOS FPGA's. The CLB itself also consists of several multiplexers.

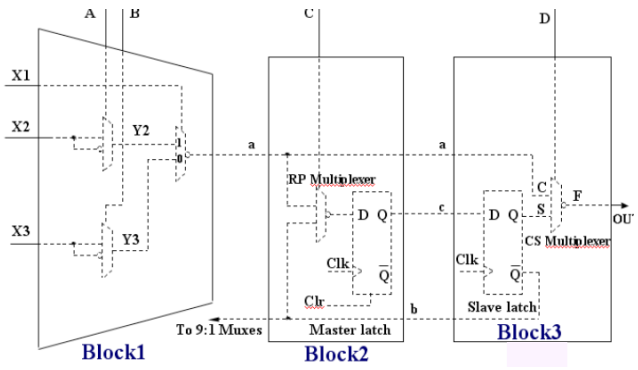

Figure 2. The XC 6200 CLB is partitioned into three blocks that each lend themselves to single CML tree realization in SiGe HBT.

Multiplexers are significant because they are readily realized in Current Steering Logic or CSL (also called Current Mode Logic or CML). CML is a preferred style of circuit for use at high frequencies since it tends to maintain constant power supply current, greatly reducing simultaneous switching noise. This can be important in mixed signal applications, including ones in which the primary function of the FPGA is to interface with A/D and D/A circuits.

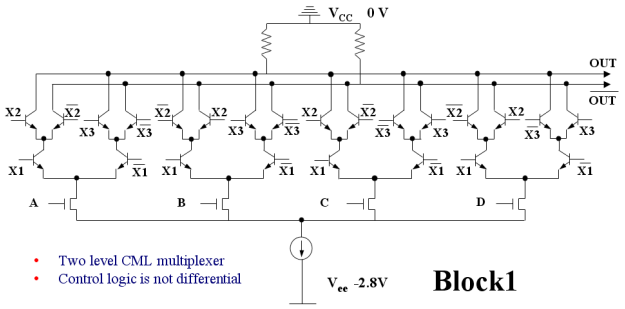

Figure 3 shows how Block 1 in Figure 2 is implemented in CML.

Full differential logic stages are stacked to provide current steering to the two output dotting rails to implement the multiplexer function. Multiplexers are ULM's in which various logic products can be selected between X1 and X2 by use of the programming signals A, B, C, and D. These latter signals are introduced by mixing FET current steering with the faster bipolar differential switches at the top of the circuit near the output dotting rails. Since the programming bits do not need to change rapidly, and only change during programming, the FET's used to implement the programming remain in saturation continuously during emulation. Only about 5% speed degradation is observed using the FET's to select the various current paths.

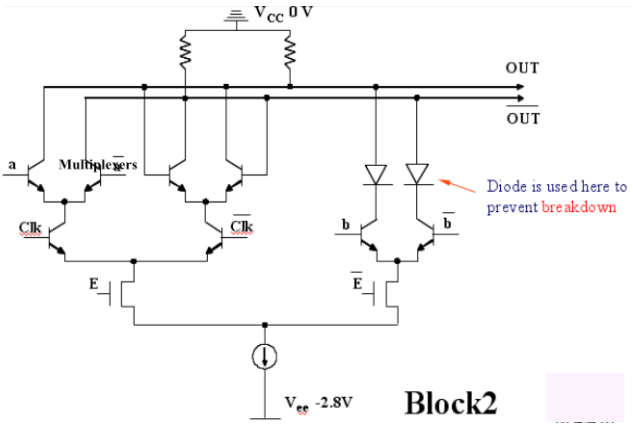

Figure 4. The CML circuit used for the Master Mux-Latch (Block 2 in the CLB).

The second block in Figure 2 is a combined multiplexer and latch implemented in a single current steering tree shown in Figure 4. This tree is interesting because it highlights an approach to dealing with a problem of increasing significance for SiGe HBT's, namely the decreasing breakdown voltage. The "b" differential switch on the right hand of the circuit diagram lacks the upper tier of differential switches on the latch side of the diagram to the left, which is enabled with the signal E. These diodes provide a voltage drop to prevent larger drops over the HBT's. The diodes do slow the swing of the output rail due to their own device capacitance. However, the slowdown is no worse than a transistor at that level in a two level multiplexer.

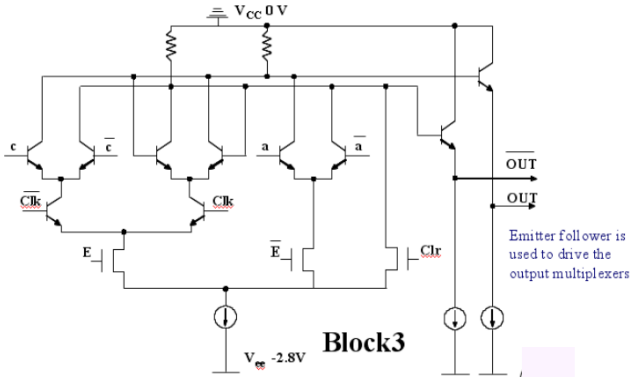

Figure 5. CLB Emitter Follower Output Stage.

The remaining Block 3 component of the CLB contains the output emitter follower for driving loads external to the CLB (there are several routing resources loading the CLB output). The base of the emitter follower also provides a breakdown voltage clamp. The HBT base collector breakdown voltage is higher than its collector emitter breakdown voltage.

1.3 Power Issues

In CML circuits current flows continuously and is steered, unless the current steering tree is powered down. The FET transistors shown in Figures 2-4 for programming can also be used to power down unused or idle current steering trees completely. A

complete XC 6200 CLB tile or logic block, including routing multiplexers, contains 24 current steering trees. It is the usual situation that not all of these current trees are active at the same time even when the CLB is being utilized. All of the trees must be turned off initially until the desired trees have been programmed to prevent initial heat overload. Because the signal voltage swing is only 250mV in CML dynamic power dissipation is negligible compared with bias current power dissipation. Consequently wherever trees can be pruned, this is done. The bias power on fully utilized trees is simply the product of current flowing through the tree and the supply voltage. This presents two methods to control power, lowering supply voltage, and varying bias current. Unlike conventional CMOS, current tree supply voltage cannot be indefinitely scaled down. However, one can attempt to confine the supply voltage to 2V in certain sections of the circuit. An example would be in routing multiplexers, which attempt to route one signal to an output. This can be achieved in two-high current trees such as shown in Figure 5.

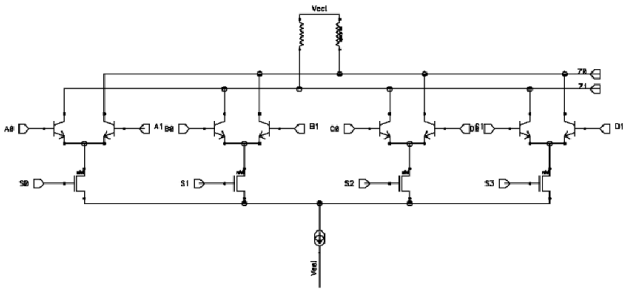

Figure 5. Two-High Routing Mux Structure using a 2V supply.

The other strategy for lowering power is to adjust current flowing through each CML tree. However, this has speed implications. The tradeoff for speed vs. power is best visualized by examining the f_T vs. Ic curve for the device. This is plotted in Figure 6, which shows the curves for various emitter AREA parameters. It is clear that to attain the highest speed offered by the SiGe HBT the bias current needs to be at the value where the peak of the f_T vs. Ic curve is located. For minimally loaded circuits the smallest AREA parameter would result in the lowest current for peak performance. However, it is evident that one can operate at lower currents and still attain a high speed of operation. Observing that the Ic axis is logarithmic one can see that operation at half speed can be attained at nearly an order of magnitude power level. However, in lowering current, the pullup resistors also have to change to maintain the logic signal swing. Current specification can be arranged over a set of current steering trees by using current mirror circuits. In this way an entire CLB can be have its speed-power tradeoff programmed with only a few bits.

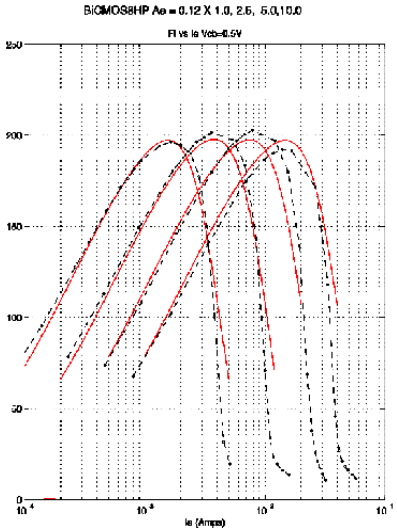

Figure 6. f_T vs. Ic Curve for IBM 8HP 210 GHz SiGe HBT.

The fact that the speed of the HBT can be varied by varying the collector current and resizing the pullup resistors suggests a scheme for implementing programmable power for each CML current tree employed in a CLB. This is shown in Figure 7. Using FET switches the power signal "Vcc-slow" can activate the appropriate pullup for slow operation, and Vcc-fast for fast operation. The "diodes" Ds1, Ds2 provide blocking action preventing Rs1 and Rs2 from shunting Rf1 and Rf2, unless both signals are activated at the same time.

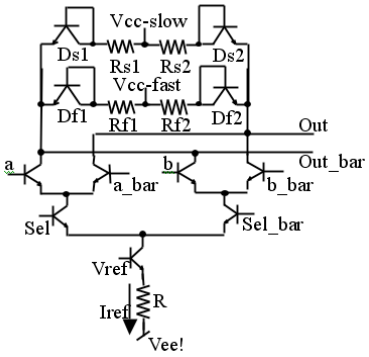

Figure 7. CML Multiplexer with two sets of pullup resistors for programmable power-speed trees.

The circuit style in Figure 7 requires numerous extra components, which increase the size of the current tree, and introduce device parasitics, which limits the fastest speed possible using this approach. Extra programming bits are used to specify the speed-power tradeoff for each CML tree, hence giving the ultimate ability to the designer for tailoring the capabilities of HBT device to its needs. It is commonplace in flexible parts such as FPGA's to have some fraction of the CLB's unused. This is just a result of the mismatch between the resources of the FPGA and those needed by the application. The resources need to exceed the needs

of the application but may have something left over. These unused resources would consume a great deal of power unless they are shut off. Use of these programmable speed-power program bits, even at a level that is more rudimentary than shown in these figures, permits turning off these unclaimed CLB's.

2. Programming and Personality Swapping

In conventional FPGA's the programming of the FET switches that personalize the part are read in serially, and locked into certain frame positions within the chip along a long shift register. In some applications, however, it is desirable to swap personalities quickly. For example one might wish to change a template signal in a correlator quickly, or the FPGA might switch to a much lower power setting if the speed is not needed. A pipeline stage can be placed at every stage along the personalization shift register. In this manner each control bit may be held fixed while a new personality bit stream is shifted in. This approximately doubles the number of flip-flops in the shift register chain. However the FET is a much smaller device than the HBT. Only a small amount of additional chip space is needed to create this operational feature. Of course the time required to shift in each personality bit sequence is lengthy as there are a lot of programming bits. However, the swapping time is on the order of one pipeline transfer (only a few nanoseconds) and is quite short, hence, as long as any one personality is needed for the duration of the shift-in time for a new personality, one personality can be executing while the next one is being shifted in, creating nearly seamless task swapping environment, and nothing terribly challenging in technology is required. With only a small additional circuitry two such personalities can be loaded and swapped back and forth in one multiplexer time. If a whole library of personalities is required, something different is needed with fast selection time, it may be possible to use a new technology, 3D chip stacking by wafer to wafer alignment and bonding [5] to provide rapid personality switching from a library of such configurations stored within such a chip stack.

3. Applications and System Speeds

The SiGe FPGA XC6200 technology discussed here is currently being developed. A 5mm x 5mm chip area is targeted for an initial prototype which is large enough to hold about a quarter of the CLB's of a XC6209 in IBM's 7HP 0.22 micron SiGe HBT BiCMOS technology. Funding limitations prevent creating the entire XC6209, but the feasibility of operation should become evident once this smaller prototype is developed. This prototype is large enough to build a 5b Fast Fourier Transform butterfly part projected to operate in pipelined fashion at 10 GHz. This requires on the order of 400 CLB's. A follow on effort is planned using IBM's new 8HP 0.13 micron SiGe HBT BiCMOS process (corresponding to figure 6, that should operate at twice that speed, and provide a wider bit width. It is estimated that the full XC 6209 part would fit inside the same 5mm x 5mm footprint.

4. CONCLUSIONS

Although the work described here is still in progress, enough is known to predict that SiGe HBT BiCMOS can provide exceptional speed in a Field Programmable Gate Array well into the 10 GHz range.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

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7. BIOSKETCH

John F. McDonald is a professor of Electrical, Computer, and Systems Engineering at the Rensselaer Polytechnic Institute in Troy, New York. He received his B.S.E.E. from MIT in 1963, and the M.Eng. and Ph.D. from Yale University in 1965 and 1969 respectively. His research currently involves exploring SiGe HBT BiCMOS technology in a variety of applications as well as 3D chip stacking technology. He is a senior member of the I.E.E.E. and a member of Sigma Xi, Tau Beta Pi and Eta Kappa Nu. The other coauthors are doctoral students is this research program or in the case of Dr. Goda, a graduate who now teaches at West Point.